DAQ

6052E/6053E User Manual

Multifunction I/O Device for
PCI/PXI™/1394 Bus Computers

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About This Manual

This manual describes the electrical and mechanical aspects of the PCI-6052E/6053E, PXI-6052E/6053E, and DAQPad-6052E and contains information concerning operation and programming.

The PCI-6052E/6053E, PXI-6052E/6053E, and DAQPad-6052E are high-performance multifunction analog, digital, and timing I/O devices for PCI, PXI, and 1394 computers. Supported functions include analog input, analog output, digital I/O, and timing I/O.

Conventions Used in This Manual

The following conventions are used in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.
♦	The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
CompactPCI	CompactPCI refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG).
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

NI-DAQ	NI-DAQ refers to the NI-DAQ driver software for Macintosh or PC compatible computers unless otherwise noted.
PC	Refers to all PC AT series computers with PCI bus unless otherwise noted.
PXI	Stands for PCI eXtensions for Instrumentation. The PXI bus is an open specification for instrumentation-specific features.
PCI E Series	Refers to switchless and jumperless enhanced MIO devices that use the DAQ-STC for timing.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ devices.

Related Documentation

The following documents contain information you can find helpful:

- *DAQ-STC Technical Reference Manual*
- National Instruments Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*
- *PCI Local Bus Specification,* Revision 2.0
- *PICMG CompactPCI 2.0 R2.1*
- *PXI Specification,* Revision 1.0

1

Introduction

This chapter describes the 6052E/6053E devices, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack your device.

About the 6052E/6053E Devices

Thank you for buying a National Instruments 6052E/6053E device. The PCI-6052E/6053E, PXI-6052E/6053E, and DAQPad-6052E are multifunction analog, digital, and timing I/O devices for PCI, PXI, and 1394 computers. Your device features two 16-bit ADCs with 16 analog inputs for 6052E or 64 analog inputs for 6053E, 16-bit DACs with voltage outputs, eight lines of TTL-compatible digital I/O, and two 24-bit counter/timers for timing I/O. Because your device has no DIP switches, jumpers, or potentiometers, it is easily software-configured and calibrated.

The PCI-6052E/6053E and PXI-6052E/6053E are completely switchless and jumperless data acquisition (DAQ) devices. This feature is made possible by the National Instruments MITE bus interface chip that connects the device to the PCI/PXI I/O bus. The MITE implements the PCI Local Bus Specification so that the interrupts and base memory addresses are all software configured.

All 6052E/6053E devices use the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamless sampling rate change.

With other DAQ devices, you cannot easily synchronize several measurement functions to a common trigger or timing event. The 6052E/6053E devices have the Real-Time System Integration (RTSI) bus to solve this problem. The RTSI bus consists of the National Instruments RTSI bus interface and a cable to route timing and trigger signals between several functions on as many as five DAQ devices in your computer.

The 6052E/6053E devices can interface to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ devices.

Detailed specifications of the 6052E/6053E devices are in Appendix A, *Specifications*.

Using PXI with CompactPCI

Using PXI compatible products with standard CompactPCI products is an important feature provided by *PXI Specification,* Revision 1.0. If you use a PXI compatible plug-in card in a standard CompactPCI chassis, you are unable to use PXI-specific functions, but you can still use the basic plug-in card functions. For example, the RTSI bus on your PXI-6052E/6053E is available in a PXI chassis but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. Your PXI-6052E/6053E works in any standard CompactPCI chassis adhering to *PICMG CompactPCI 2.0 R2.1*.

What You Need to Get Started

To set up and use your 6052E/6053E device, you need the following:

- ❑ One of the following:
  - PCI-6052E/6053E
  - PXI-6052E/6053E
  - DAQPad-6052E for 1394
- ❑ *6052E/6053E User Manual*
- ❑ One of the following software packages and documentation:
  - LabVIEW for Macintosh
  - LabVIEW for Windows
  - Measure

  - Measurement Studio
  - NI-DAQ for Macintosh
  - NI-DAQ for PC Compatibles
  - VirtualBench

- ❑ Your computer

Software Programming Choices

You have several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use National Instruments application software or NI-DAQ.

National Instruments Application Software

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to NI-DAQ software.

Measurement Studio, which contains LabWindows/CVI and measurement tools for Visual C++ and Visual Basic, features interactive graphics, configurable user interface controls, and language-customized interfaces to the NI-DAQ software through standard ANSI C functions, C++ classes, and ActiveX controls. With Measurement Studio, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using LabVIEW, Measurement Studio, or VirtualBench software greatly reduces the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages or National Instruments application software, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

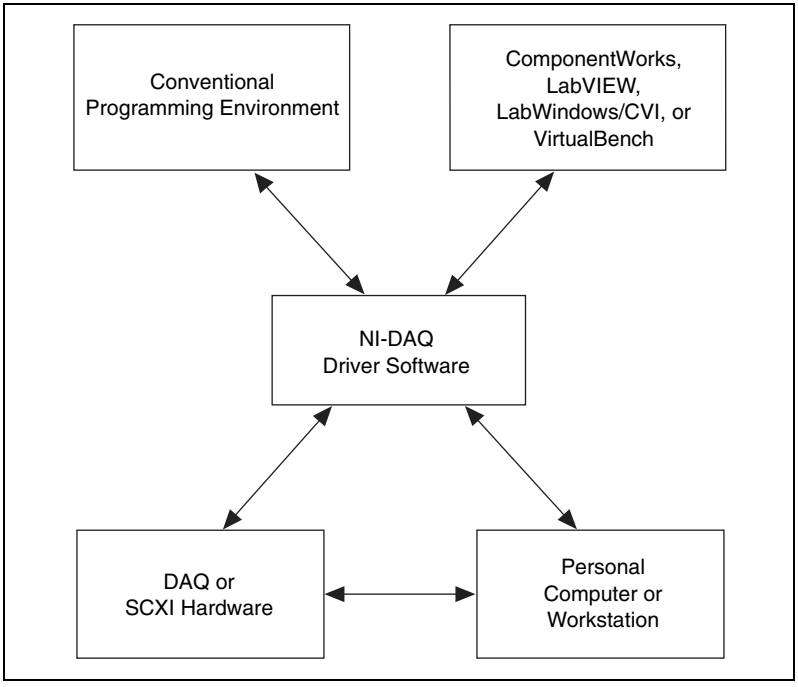


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Optional Equipment

National Instruments offers a variety of products to use with your device, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50- and 68-pin screw terminals
- RTSI bus cables
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For specific information about these products, refer to your National Instruments catalogue or Web site or call the office nearest you.

2

Installation and Configuration

This chapter explains how to install and configure your device.

Software Installation

Install your software before you install your device. Refer to the appropriate release notes indicated below for specific instructions on the software installation sequence.

If you are using LabVIEW, Measurement Studio, other National Instruments application software packages, or the NI-DAQ driver software, refer to the appropriate release notes. After you have installed your application software, refer to your NI-DAQ release notes and follow the instructions given there for your operating system and application software package.

Unpacking

Your device is shipped in an antistatic package to prevent electrostatic damage. Electrostatic discharge can damage several components on the device. To avoid such damage in handling the device, take the following precautions:

- Remove the device from the package and inspect the device for loose components or any other sign of damage. Notify National Instruments if the device appears damaged in any way. Do *not* install a damaged device into your computer.
- *Never* touch the exposed pins of connectors.

Hardware Installation

You can install your PCI-6052E/6053E or PXI-6052E/6053E in any available 5 V PCI or PXI slot, respectively, in your computer. However, to achieve best noise performance, leave as much room as possible between the PCI-6052E/6053E and PXI-6052E/6053E and other devices. You can connect your DAQPad-6052E to any available 1394 port. The following

are general installation instructions. Consult your computer user manual or technical reference manual for specific instructions and warnings.

- PCI-6052E/6053E
  1. Turn off and unplug your computer.
  2. Remove the top cover of your computer.
  3. Remove the expansion slot cover on the back panel of the computer.
  4. Touch any metal part of your computer chassis to discharge any static electricity that might be on your clothes or body.
  5. Insert your device into a 5 V PCI slot. Gently rock the device to ease it into place. It can be a tight fit, but *do not force* the device into place.
  6. If required, screw the mounting bracket of the PCI-6052E/6053E to the back panel rail of the computer.
  7. Visually verify the installation.
  8. Replace the cover.
  9. Plug in and turn on your computer.

  The PCI-6052E/6053E is now installed.

- PXI-6052E/6053E
  1. Turn off and unplug your computer.
  2. Choose an unused PXI slot in your system. For maximum performance, the PXI-6052E/6053E has an onboard DMA controller that can only be used if the device is installed in a slot that supports bus arbitration, or bus master cards. National Instruments recommends installing the PXI-6052E/6053E in such a slot. The PXI specification requires all slots to support bus master cards, but the CompactPCI specification does not. If you install in a CompactPCI non-master slot, you must disable the PXI-6052E/6053E onboard DMA controller using software.
  3. Remove the filler panel for the slot you have chosen.
  4. Insert the PXI-6052E/6053E into a 5 V PXI slot. Use the injector/ejector handle to fully insert the device into the chassis.
  5. Screw the front panel of the PXI-6052E/6053E to the front panel mounting rail of the system.
  6. Plug in and turn on your computer.

  The PXI-6052E/6053E is now installed.

- DAQPad-6052E for 1394

Note If you are *not* using the BP-1 battery pack, follow the instructions in the next section. If you are using the BP-1 battery pack, follow the installation instructions in your BP-1 installation guide and disregard step 1 in this section.

1. Connect the power cord to the wall outlet and the DAQPad device.
2. Connect the 1394 cable from the computer or any other 1394 device to the port on your DAQPad device. Your computer should detect your DAQPad device immediately. When the computer recognizes your DAQPad devicel, the COM LED on the front panel will blink. Refer to the *Configuration* section for information on LEDs.
3. The power LED should be on. Refer to the *Configuration* section for information on LEDs.
4. Configure your DAQPad device and any accessories with NI-DAQ.

Your DAQPad-6052E for 1394 is now installed. You are now ready to configure your hardware and software.

Configuration

- PCI-6052E/6053E, PXI-6052E/6053E

  The PCI-6052E/6053E and PXI-6052E/6053E are completely software configurable. You must perform two types of configuration on the PCI-6052E/6053E and PXI-6052E/6053E—bus-related and data acquisition-related configuration.

  The PCI-6052E/6053E and PXI-6052E/6053E are fully compatible with the industry-standard *PCI Local Bus Specification,* Revision 2.0, and *PXI Specification,* Revision 1.0. This allows the PCI/PXI system to automatically perform all bus-related configurations and requires no user interaction. Bus-related configuration includes setting the device base memory address and interrupt channel.

  You can modify data acquisition-related configuration settings such as analog input polarity and range, analog input mode, and others through application level software, such as NI-DAQ, ComponentWorks, LabVIEW, LabWindows/CVI, and VirtualBench.

- DAQPad-6052E for 1394

  The DAQPad-6052E for 1394 is a completely software-configurable, hot Plug and Play instrument. The Plug and Play services query the instrument and allocate the required resources. The operating system enables the instrument for operation. Refer to your software documentation for more information.

  The DAQPad-6052E for 1394 is equipped with two LEDs to help you determine the state of your device:

  - Power LED
    - Power LED–off—no power is being provided to the device. Either the power cord is unplugged, or the power source is broken.
    - Power LED–dim—the device is receiving power, but is not connected to an active 1394 port.
    - Power LED–on—the device is receiving power and is connected to an active 1394 port.
  - Communications LED—the COM LED blinks whenever the device sends or receives any commands or data. This LED should blink once when you first plug in your device. If you are transferring a lot of data, this light should be on or blinking continuously.

  Refer to your software documentation for configuration instructions.

3

Hardware Overview

This chapter presents an overview of the hardware functions on your 6052E/6053E device.

Figure 3-1 shows a block diagram for the 6052E/6053E devices.

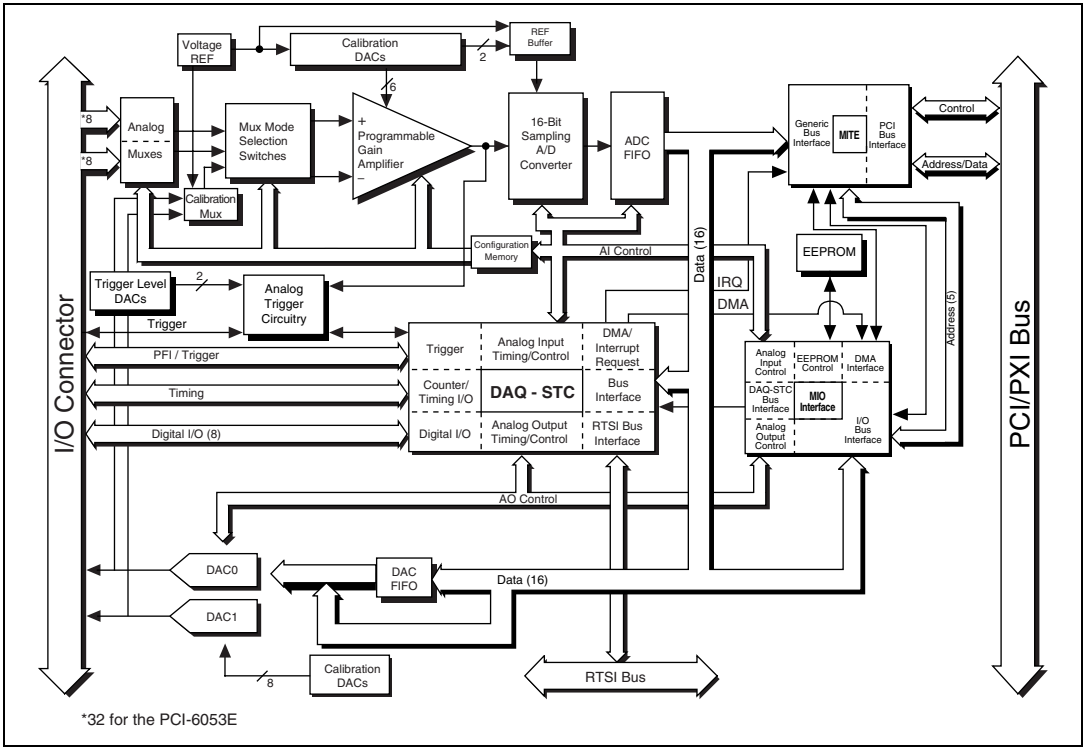


Figure 3-1. PCI and PXI Block Diagram

Analog Input

The analog input section of the 6052E/6053E is software configurable. You can select different analog input configurations through application software designed to control your device. The following sections describe in detail each of the analog input categories.

Input Mode

The PCI devices have three different input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations provide up to 16 channels on the 6052E or 64 channels on the 6053E. The DIFF input configuration provides up to eight channels on the 6052E or 32 channels on the 6053E. Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially-configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

Table 3-1. Available Input Configurations for the 6052E/6053E Devices

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog input lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to analog input sense (AISENSE).

For more information about the three types of input configuration, refer to the *Analog Input Signal Connections* section in Chapter 4, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

Input Polarity and Input Range

The 6052E/6053E devices have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. So, the device has a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V).

Polarity and range settings can be programmed on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on the 6052E/6053E devices increases the overall flexibility of each device by matching the input signal ranges to those that the ADC can accommodate. Each device has gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and is suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Precision*
0 to +10 V	1.0	0 to +10 V	153 µV
	2.0	0 to +5 V	76.3 µV
	5.0	0 to +2 V	30.5 µV
	10.0	0 to +1 V	15.3 µV
	20.0	0 to +500 mV	7.63 µV
	50.0	0 to +200 mV	3.05 µV
	100.0	0 to +100 mV	1.53 µV
–5 to +5 V	0.5	–10 to +10 V	305 µV
	1.0	–5 to +5 V	153 µV
	2.0	–2.5 to +2.5 V	76.3 µV
	5.0	–1 to +1 V	30.5 µV
	10.0	–500 to +500 mV	15.6 µV
	20.0	–250 to +250 mV	7.63 µV
	50.0	–100 to +100 mV	3.05 µV
	100.0	–50 to +50 mV	1.53 µV

* The value of 1 LSB of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

The input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but can result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal is not below 0 V, unipolar input polarity is best. However, if the signal is negative, you get inaccurate readings if you use unipolar input polarity.

Multichannel Scanning Considerations

The 6052E/6053E can scan multiple channels at the same maximum rate as its single-channel rate; however, pay careful attention to the settling time. The settling time is independent of the selected gain, even at the maximum sampling rate. The settling time for the very high-speed devices is gain dependent, which can affect the useful sampling rate for a given gain. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times.

When scanning among channels at various gains, the settling times can increase. When the PGIA switches to a higher gain, the signal on the previous channel can be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 16-bit device to settle within 0.0015% (15 ppm or 1 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. It can take as long as 200 µs for the circuitry to settle this much. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals due to a phenomenon called *charge injection*, where the analog input multiplexer injects a small amount of charge into each signal source when that source is selected. If the impedance of the source is not low enough,

the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ to perform high-speed scanning.

Due to problems with settling times, multichannel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Output

The 6052E/6053E devices supply two channels of analog output voltage at the I/O connector. The reference and range for the analog output circuitry is software-selectable. The reference can be either internal or external, whereas the range can be either bipolar or unipolar.

Analog Output Reference Selection

You can connect each D/A converter (DAC) to an internal reference of 10 V or to the external reference signal connected to the EXTREF pin on the I/O connector. This signal applied to EXTREF should be within ±11 V. You do not need to configure both channels for the same mode.

Analog Output Polarity Selection

You can configure each analog output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. V_{ref} is the voltage reference used by the DACs in the analog output circuitry and can be either the +10 V onboard reference or an externally supplied reference within ±11 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that any data written to that DAC is interpreted as two's complement format. In two's complement mode, data values written to the analog output channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary format. In straight binary mode, data values written to the analog output channel range must be positive.

Analog Output Reglitch

In normal operation, a DAC output glitches whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit does *not* eliminate the glitches; it only makes them more uniform in size.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a data acquisition sequence, the 6052E/6053E devices also support analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-2. The trigger-level range for the direct analog channel is in 4.9 mV steps. The range for the post-PGIA trigger selection is the full-scale range of the selected channel. The resolution is that range divided by 4,096.

Note The PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input via software.

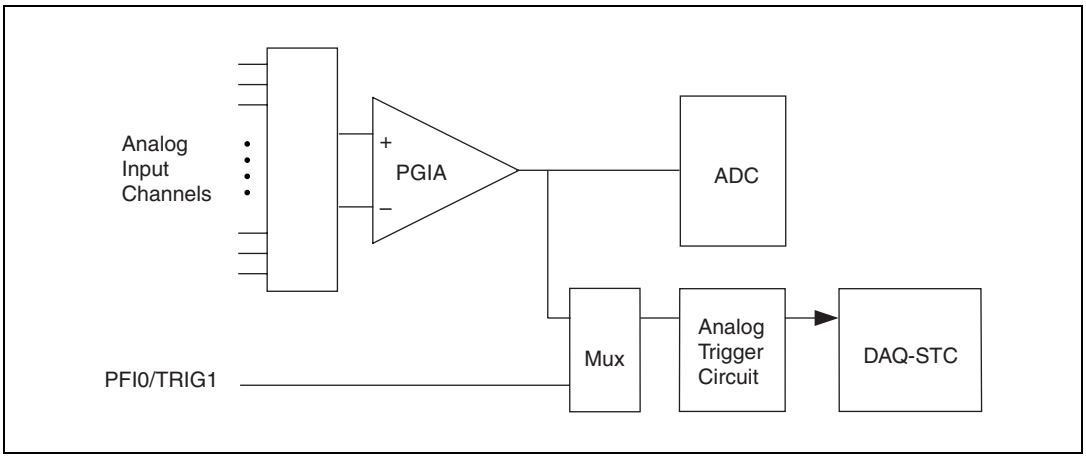


Figure 3-2. Analog Trigger Block Diagram

There are five analog triggering modes available, as shown in Figures 3-3 through 3-7. You can set **lowValue** and **highValue** independently in software.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is unused.

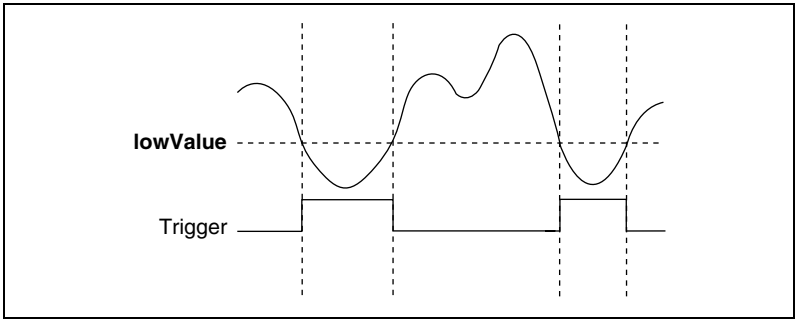


Figure 3-3. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is unused.

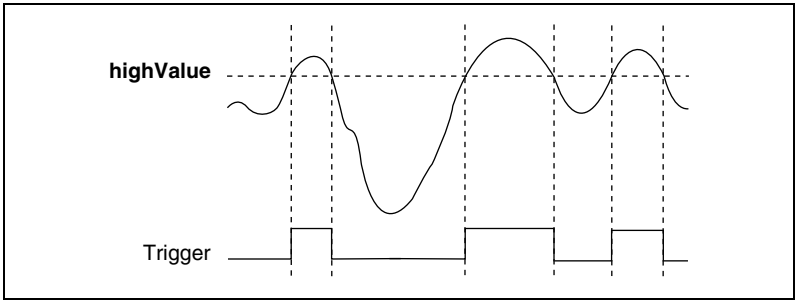


Figure 3-4. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue.**

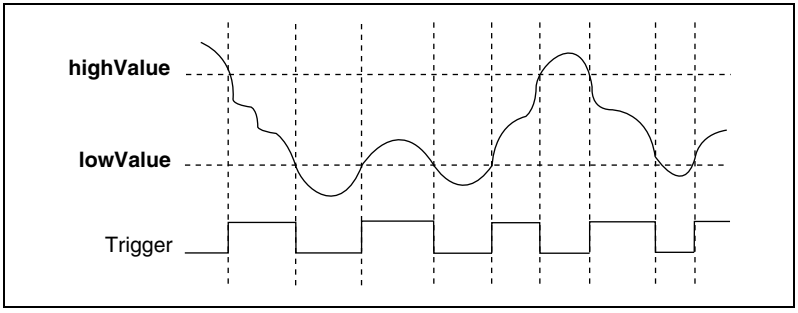


Figure 3-5. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**.

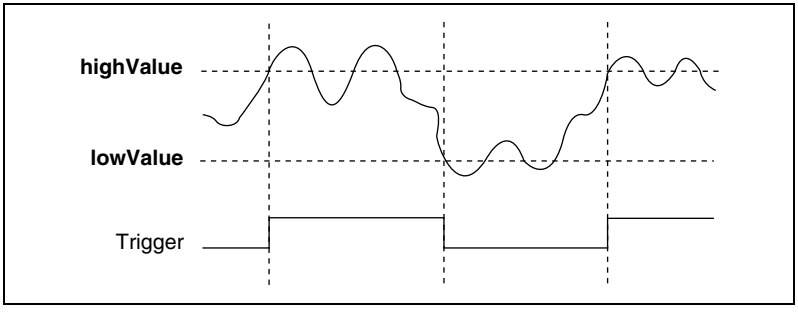


Figure 3-6. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue.**

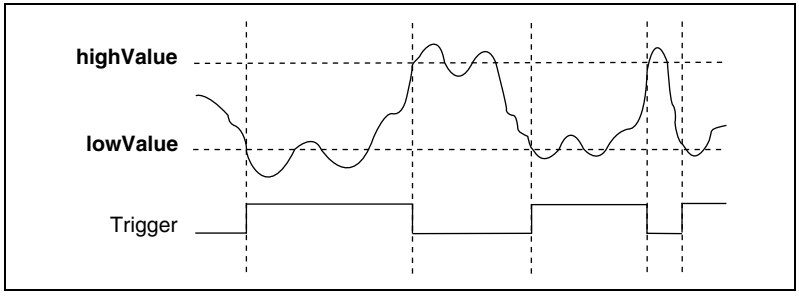


Figure 3-7. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the analog input signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the analog input, analog output, and general-purpose counter/timer sections. For example, the analog input section can be configured to acquire *n* scans after the analog input signal crosses a specific threshold. The analog output section can be configured to update its outputs whenever the analog input signal crosses a specific threshold.

Digital I/O

The 6052E/6053E devices contain eight lines of digital I/O for general-purpose use. You can individually software-configure each line for either input or output. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other devices or external circuitry. Your device uses the RTSI bus to interconnect timing signals between devices, and the Programmable Function Input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable your device to both control and be controlled by other devices and circuits.

There are a total of 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. Figure 3-8 shows an example of the signal routing multiplexer controlling the CONVERT* signal.

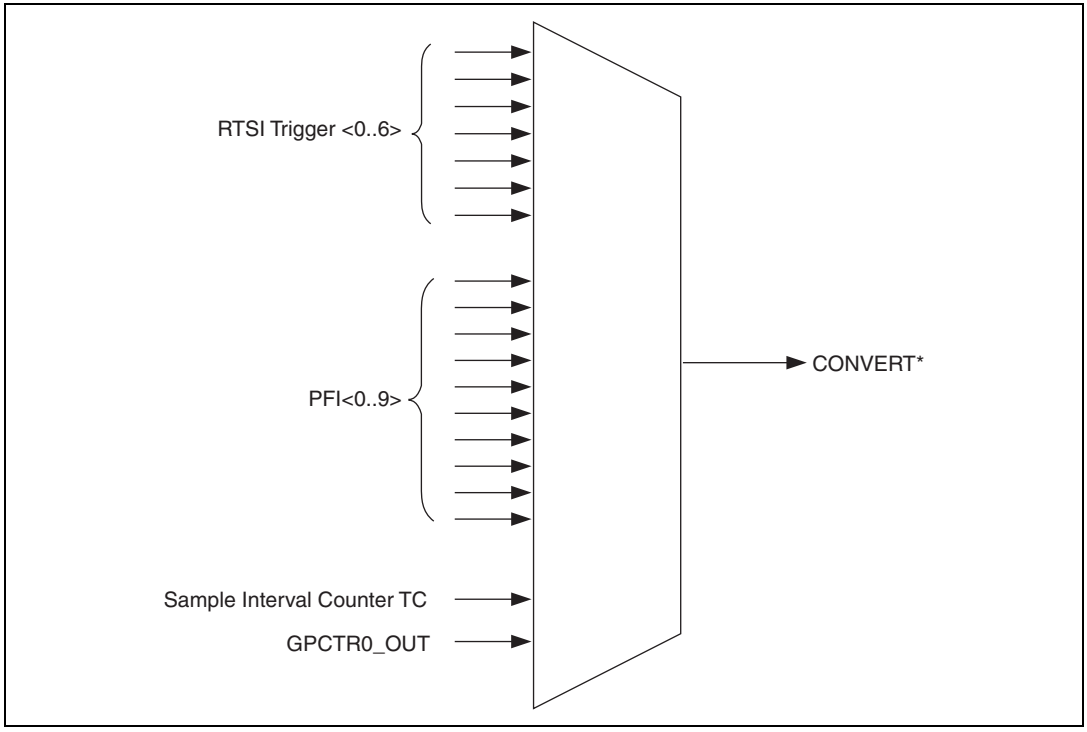


Figure 3-8. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section later in this chapter, and on the PFI pins, as indicated in Chapter 4, *Signal Connections*.

Programmable Function Inputs

Ten PFI signals are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFI pins as the external source for a given timing signal. It is important to note that any of the PFI pins can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many functions performed by the 6052E/6053E devices require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

The 6052E/6053E device can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, you can also program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software selectable. The PCI-6052E/6053E have separate connectors for the RTSI bus. The PXI-6052E/6053E uses signals on the PXI backplane for RTSI Clock. The RTSI Clock signal uses the PXI trigger <7> line for this connection.

RTSI Triggers

The RTSI trigger lines on the RTSI bus provide a very flexible interconnection scheme for any 6052E/6053E device sharing the RTSI bus. The PCI-6052E/6053E and PXI-6052E/6053E have seven trigger lines. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-9. For the PXI-6052E/6053E,

the RTSI trigger lines connect to other devices through the PXI bus on the PXI backplane. RTSI<0..5> connect to PXI Trigger<0..5>, respectively. RTSI<6> connects to PXI Star. This signal connection scheme is shown in Figure 3-10.

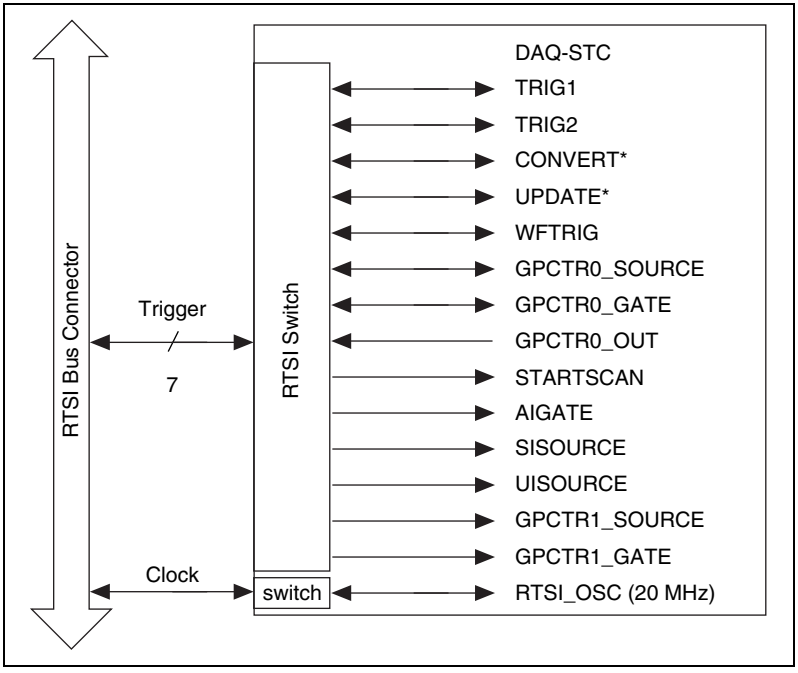


Figure 3-9. PCI RTSI Bus Signal Connection

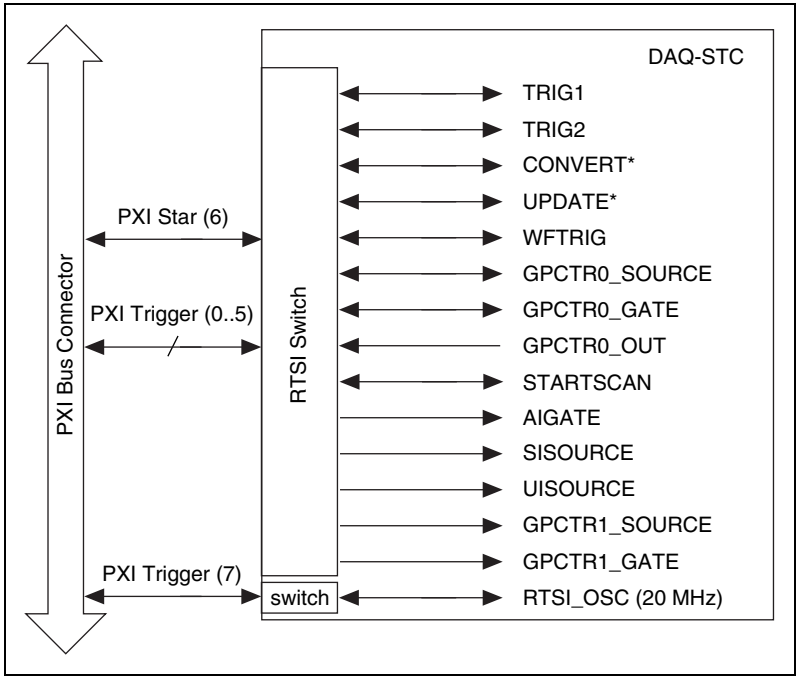


Figure 3-10. PXI RTSI Bus Signal Connection

Refer to the *Timing Connections* section of Chapter 4, *Signal Connections*, for a description of the signals shown in Figures 3-9 and 3-10.

4

Signal Connections

This chapter describes how to make input and output signal connections to your device via the device I/O connector.

The I/O connector has 68 pins on the 6052E that you can connect to 68-pin accessories with the SH6868 shielded cable or the R6868 ribbon cable. You can connect your device to 50-pin signal conditioning modules and terminal blocks with the SH6850 shielded cable or R6850 ribbon cable.

The I/O connector for 6053E has 100 pins that you can connect to 100-pin accessories with the SH100100 shielded cable. With the SH1006868 shielded cable, you can connect your device to the 68-pin accessories. With the R1005050 ribbon cable, you can connect your device to 50-pin accessories.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector. Figure 4-2 shows the pin assignments for the 100-pin I/O connector. Refer to Appendix B, *Custom Cabling and Optional Connectors*, for the pin assignments of the 50-pin connector. A signal description follows the figures.

Caution Connections that exceed any of the maximum ratings of input or output signals on the 6052E/6053E device can damage the device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-3. National Instruments is *not* liable for any damages resulting from such signal connections.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure 4-1. I/O Connector Pin Assignment for 6052E

AIGND	1	51	ACH16
AIGND	2	52	ACH24
ACH0	3	53	ACH17
ACH8	4	54	ACH25
ACH1	5	55	ACH18
ACH9	6	56	ACH26
ACH2	7	57	ACH19
ACH10	8	58	ACH27
ACH3	9	59	ACH20
ACH11	10	60	ACH28
ACH4	11	61	ACH21
ACH12	12	62	ACH29
ACH5	13	63	ACH22
ACH13	14	64	ACH30
ACH6	15	65	ACH23
ACH14	16	66	ACH31
ACH7	17	67	ACH32
ACH15	18	68	ACH40
AISENSE	19	69	ACH33
DAC0OUT	20	70	ACH41
DAC1OUT	21	71	ACH34
EXTREF	22	72	ACH42
AOGND	23	73	ACH35
DGND	24	74	ACH43
DIO0	25	75	AISENSE2
DIO4	26	76	AIGND
DIO1	27	77	ACH36
DIO5	28	78	ACH44
DIO2	29	79	ACH37
DIO6	30	80	ACH45
DIO3	31	81	ACH38
DIO7	32	82	ACH46
DGND	33	83	ACH39
+5 V	34	84	ACH47
+5 V	35	85	ACH48
SCANCLK	36	86	ACH56
EXTSTROBE*	37	87	ACH49
PFI0/TRIG1	38	88	ACH57
PFI1/TRIG2	39	89	ACH50
PFI2/CONVERT*	40	90	ACH58
PFI3/GPCTR1_SOURCE	41	91	ACH51
PFI4/GPCTR1_GATE	42	92	ACH59
GPCTR1_OUT	43	93	ACH52
PFI5/UPDATE*	44	94	ACH60
PFI6/WFTRIG	45	95	ACH53
PFI7/STARTSCAN	46	96	ACH61
PFI8/GPCTR0_SOURCE	47	97	ACH54
PFI9/GPCTR0_GATE	48	98	ACH62
GPCTR0_OUT	49	99	ACH55
FREQ_OUT	50	100	ACH63

Figure 4-2. I/O Connector Pin Assignment for the 6053E

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 4-1 shows the J2 pins used by your PXI-6052E/6053E. Your PXI device is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and not ever enabled. Damage can result if these lines are driven by the sub-bus.

Table 4-1. Pins Used by the PXI-6052E/6053E

PXI-6052E/6053E Signal	PXI Pin Name	PXI J2 Pin Number
RTSI<0..5>	PXI Trigger<0..5>	B16, A16, A17, A18, B18, C18
RTSI 6	PXI Star	D17
RTSI Clock	PXI Trigger 7	E16
Reserved	LBL<0..3>	C20, E20, A19, C19
Reserved	LBR<0..12>	A21, C21, D21, E21, A20, B20, E15, A3, C3, D3, E3, A2, B2

Table 4-2. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your device.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
ACH<16.63>	AIGND	Input	Analog Input Channels 16 through 63 (6053E only)—Each channel pair, ACH<*i*, *i*+8> (i=16..23, 32..39, 48..55) can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
AISENSE2	AIGND	Input	Analog Input Sense (6053E only)—This pin serves as the reference node for any of channels ACH <16.63> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
EXTREF	AOGND	Input	External Reference—This is the external reference input for the analog output circuitry.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on your 6052E/6053E device.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your 6052E/6053E device.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO 6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.

Table 4-2. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is either one of the Programmable Function Inputs (PFIs) or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section in this chapter. The hardware analog trigger is explained in the *Analog Trigger* section in Chapter 3, *Hardware Overview*.
		Output	As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.

Table 4-2. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-3. I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..63>	AI	100 GΩ in parallel with 100 pF	± 25/15	—	—	—	±200 pA
AISENSE, AISENSE2	AI	100 GΩ in parallel with 100 pF	± 25/15	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	20 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	20 V/µs	—
EXTREF	AI	10 kΩ	± 25/15	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	AI DIO	10 kΩ	±35 V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	9 kΩ pu and 10 kΩ pd
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-3. I/O Signal Summary (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}-0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog InputDIO = Digital Input/Outputpu = pullup
AO = Analog OutputDO = Digital OutputAI/DIO = Analog/Digital Input/Output

* Indicates active low

Note: The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value can range between 17 kΩ and 100 kΩ.

Analog Input Signal Connections

- PCI-6052E and PXI-6052E

  The analog input signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are connected to the 16 analog input channels of your 6052E device. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the device PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

- PCI-6053E and PXI-6053E

  The analog input signals are ACH<0..63>, AISENSE, AISENSE2, and AIGND. The ACH<0..63> signals are tied to the 64 analog input channels of the devices. In single-ended mode, signals connected to ACH<0..63> are routed to the positive input of the PGIA. In differential mode, signals connected to ACH<0..7, 16..23, 32..39, 48..55> are routed to the positive input of the PGIA, and signals connected to ACH<8..15, 24..31, 40..47, 56..63> are routed to the negative input of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage your device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-3.

In NRSE mode, the AISENSE signal is connected internally to the negative input of the PGIA when their corresponding channels are selected. In DIFF and RSE modes, this signal is left unconnected.

AIGND is an analog input common signal that is routed directly to the ground tie point on your device. You can use this signal for a general analog ground tie point to your device if necessary.

Connection of analog input signals to your device depends on the configuration of the analog input channels you are using and the type of input signal source. With the different configurations, you can use the PGIA in different ways. Figure 4-3 shows a diagram of the PGIA.

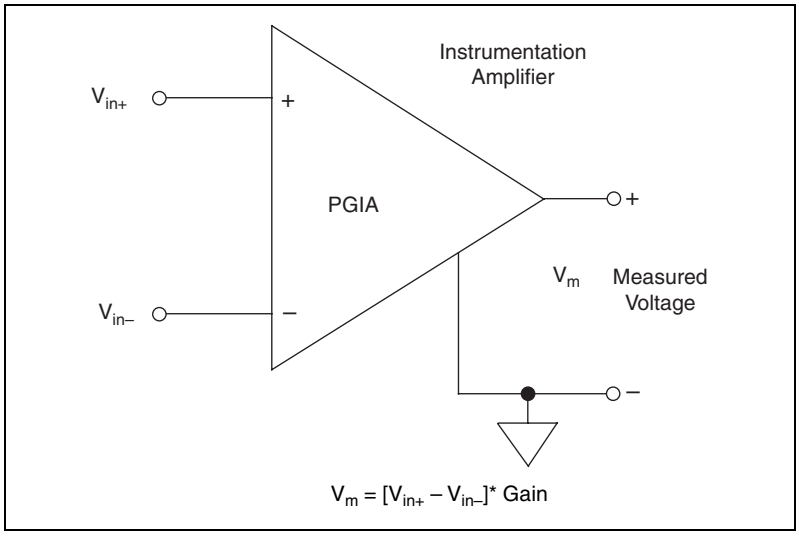


Figure 4-3. PGIA

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to your device. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. Your device A/D converter (ADC) measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the device. If you have a floating source, you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with

bias resistors, see the *Differential Connections for Nonreferenced or Floating Signal Sources* section in this chapter. If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to your device analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

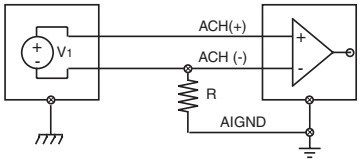
A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the device, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

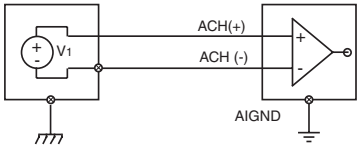
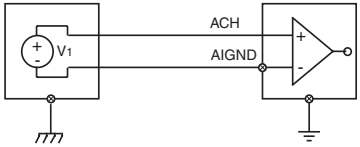
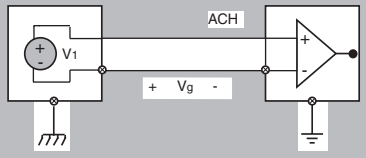
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference can appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

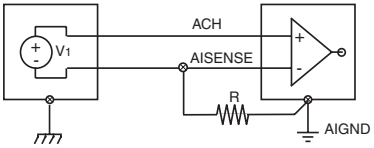
Input Configurations

You can configure your device for one of three input modes—NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 4-4 summarizes the recommended input configuration for both types of signal sources.

<table>
<tr><td rowspan="2"></td><td colspan="2">Signal Source Type</td></tr>
<tr><td>Floating Signal Source
(Not Connected to Building Ground)</td><td>Grounded Signal Source</td></tr>
<tr><td>Input</td><td>Examples
• Ungrounded Thermocouples
• Signal conditioning with isolated outputs
• Battery devices</td><td>Examples
• Plug-in instruments with nonisolated outputs</td></tr>
<tr><td>Differential (DIFF)</td><td> 

See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended — Ground Referenced (RSE)</td><td> 
</td><td>NOT RECOMMENDED
 

Ground-loop losses, Vg, are added to measured signal</td></tr>
<tr><td>Single-Ended — Nonreferenced (NRSE)</td><td> 

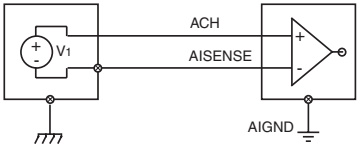
See text for information on bias resistors.</td><td> 
</td></tr>
</table>

Figure 4-4. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the device analog input signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight analog input channels are available. You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the 6052E/6053E device are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-5 shows how to connect a ground-referenced signal source to a channel on the 6052E/6053E device configured in DIFF input mode.

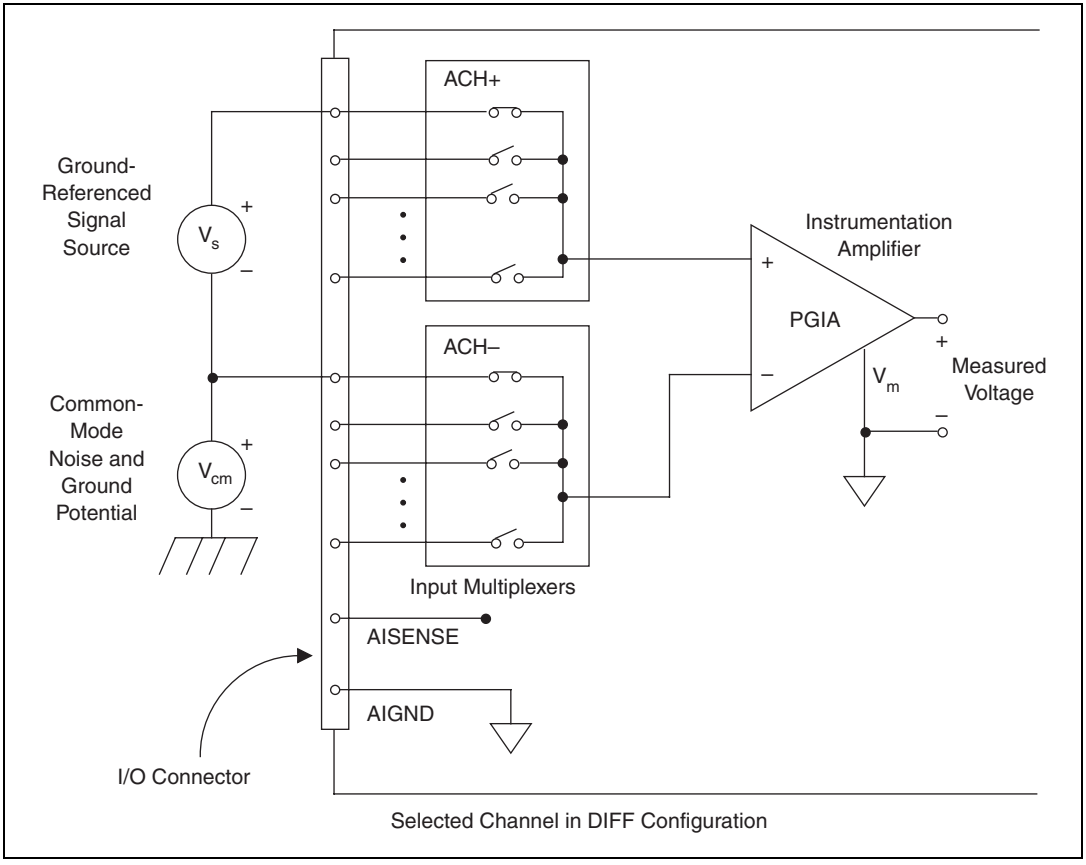


Figure 4-5. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in Figure 4-5.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-6 shows how to connect a floating signal source to a channel on the 6052E/6053E device configured in DIFF input mode.

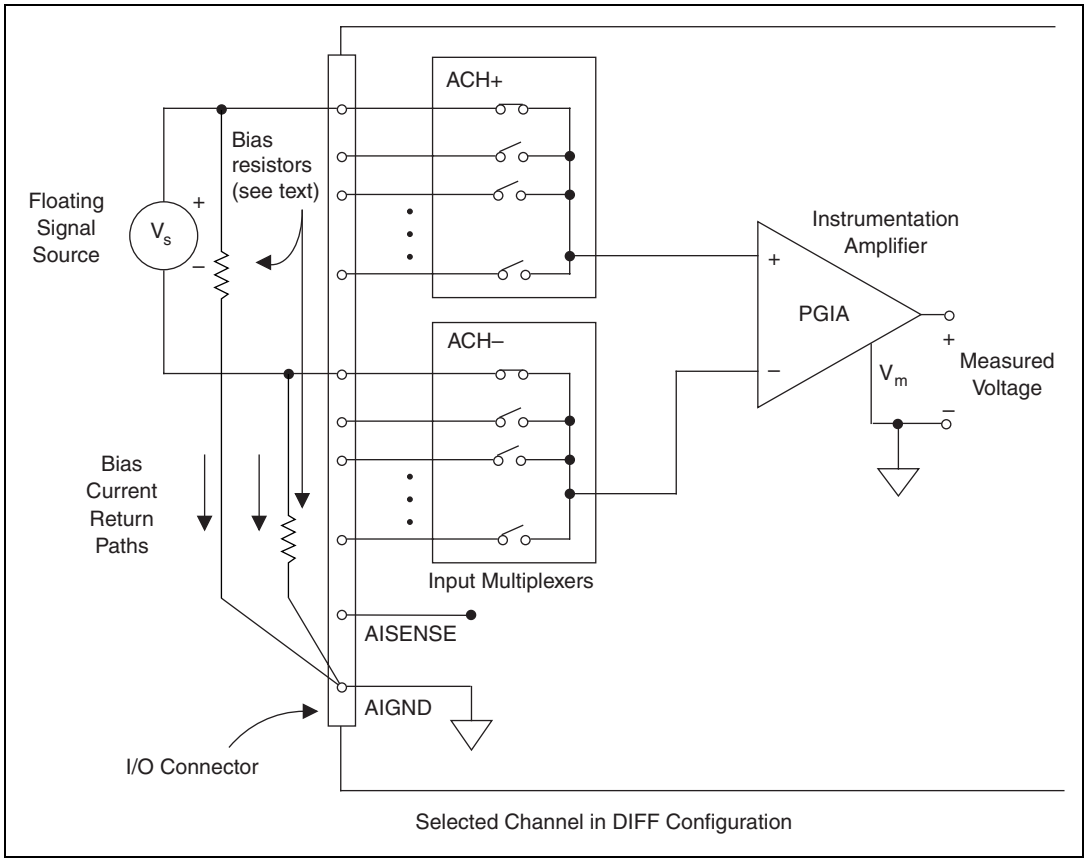


Figure 4-6. Differential Input Connections for Nonreferenced Signals

Figure 4-6 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA. The PGIA will then saturate, causing erroneous readings. You must reference the source to AIGND. The easiest way is to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors at all. This

connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-6. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the analog input signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels on the 6052E and 64 input channels on the 6053E are available. You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the 6052E/6053E are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

Using your software, you can configure the 6052E/6053E channels for two different types of single-ended connections—RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the 6052E/6053E provides the reference ground point for the external signal. The NRSE input configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point. The device should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-7 shows how to connect a floating signal source to a channel on the 6052E/6053E configured for RSE mode.

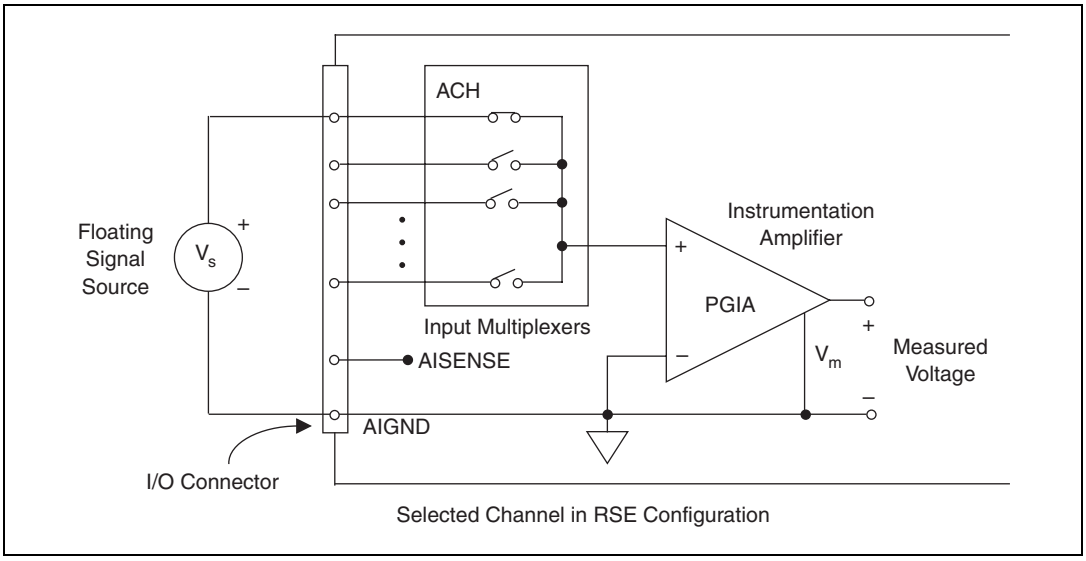


Figure 4-7. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your device in the NRSE input configuration. The signal is then connected to the positive input of the PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the 6052E/6053E ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of the 6052E/6053E were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-8 shows how to connect a grounded signal source to a channel on the 6052E/6053E configured for NRSE mode.

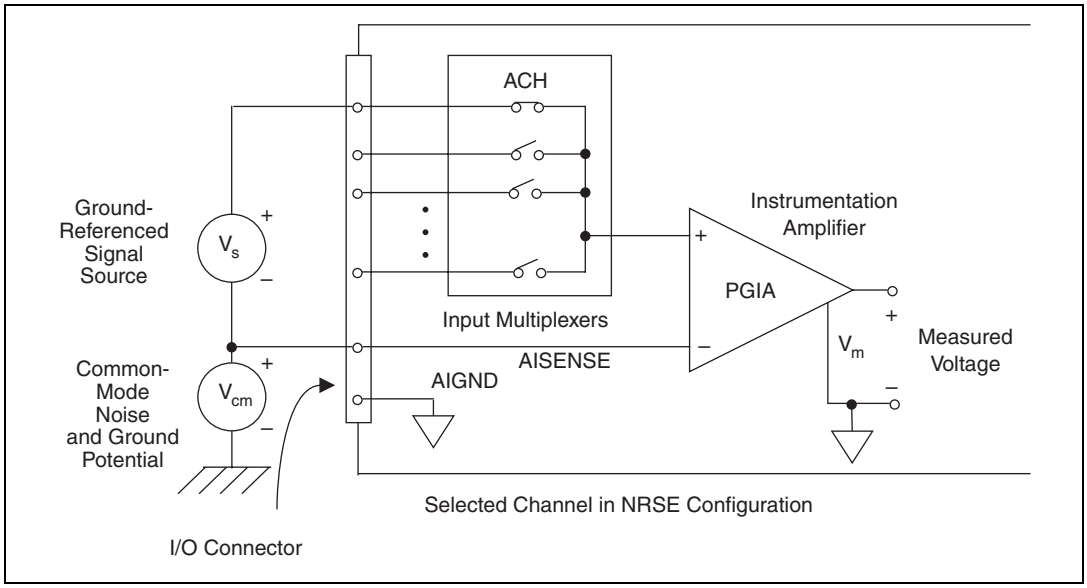


Figure 4-8. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-5 and 4-8 show connections for signal sources that are already referenced to some ground point with respect to the 6052E/6053E. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within ±11 V of AIGND.

Analog Output Signal Connections

The analog output signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

DAC0OUT is the voltage output signal for analog output channel 0. DAC1OUT is the voltage output signal for analog output channel 1.

EXTREF is the external reference input for both analog output channels. You must configure each analog output channel individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. If you do not specify an external reference, the channel will use the internal reference. Analog output configuration options are explained in the *Analog Output* section in Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both analog output channels and the external reference signal.

Figure 4-9 shows how to make analog output connections and the external reference input connection to your device.

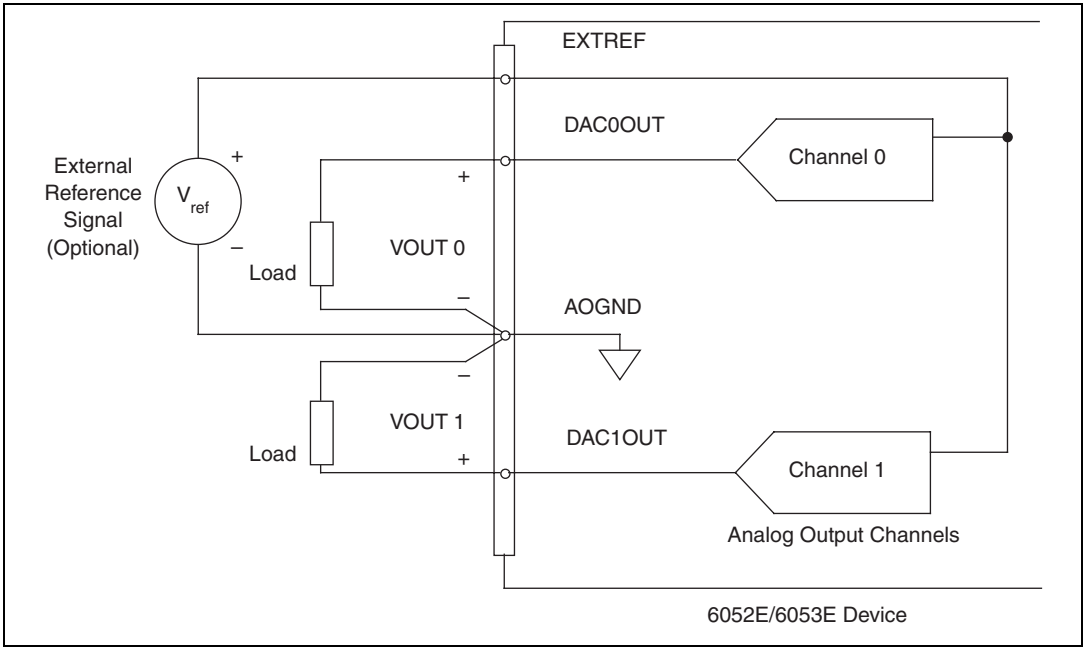


Figure 4-9. Analog Output Connections

The external reference signal can be either a DC or an AC signal. The device multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3 can damage your device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections.

Figure 4-10 shows signal connections for three typical digital I/O applications. Figure 4-10 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state

of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

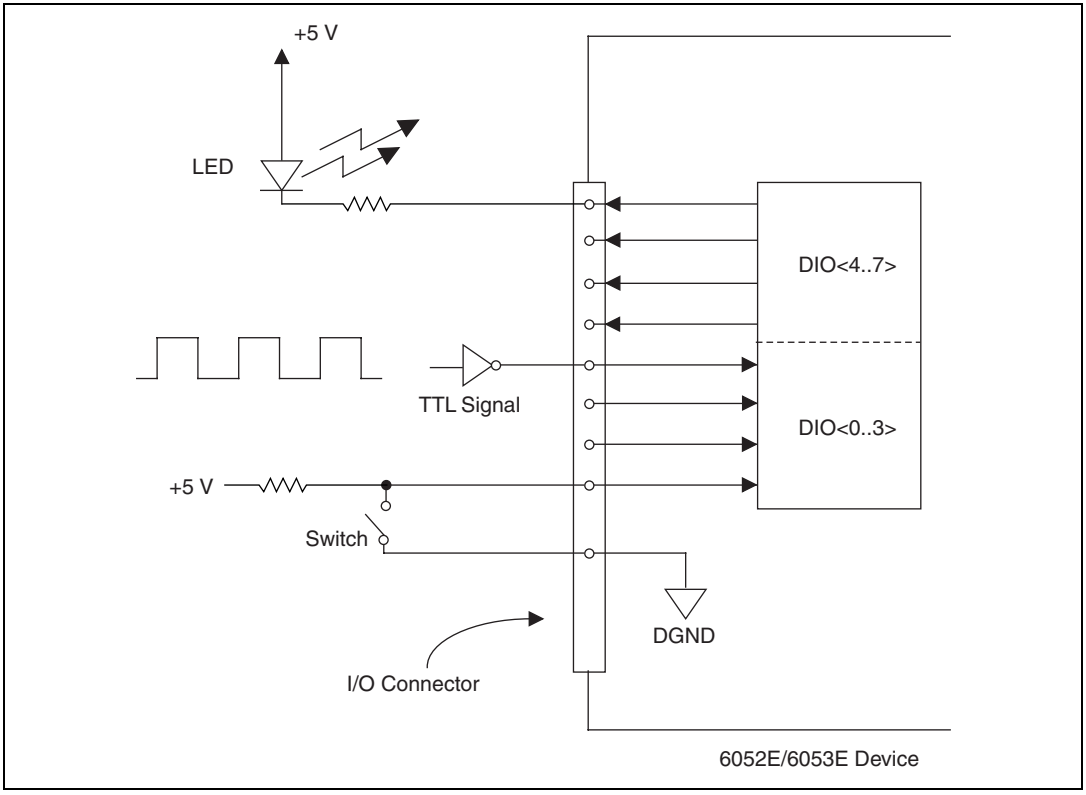


Figure 4-10. Digital I/O Connections

Power Connections

Two pins on the I/0 connector supply +5 V from the computer power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The fuse power rating is +4.65 to +5.25 VDC at 1 A.

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the device or any other device. Doing so can damage the device and the computer. National Instruments is *not* liable for damages resulting from such a connection.

Timing Connections

Caution Exceeding the maximum input voltage ratings that are listed in Tables 4-3 can damage your device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections.

All external control over the timing of your device is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The DAQ signals are explained in the *DAQ Timing Connections* section in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section in this chapter.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-11, which shows how to connect an external TRIG1 source and an external CONVERT* source to two 6052E/6053E PFI pins.

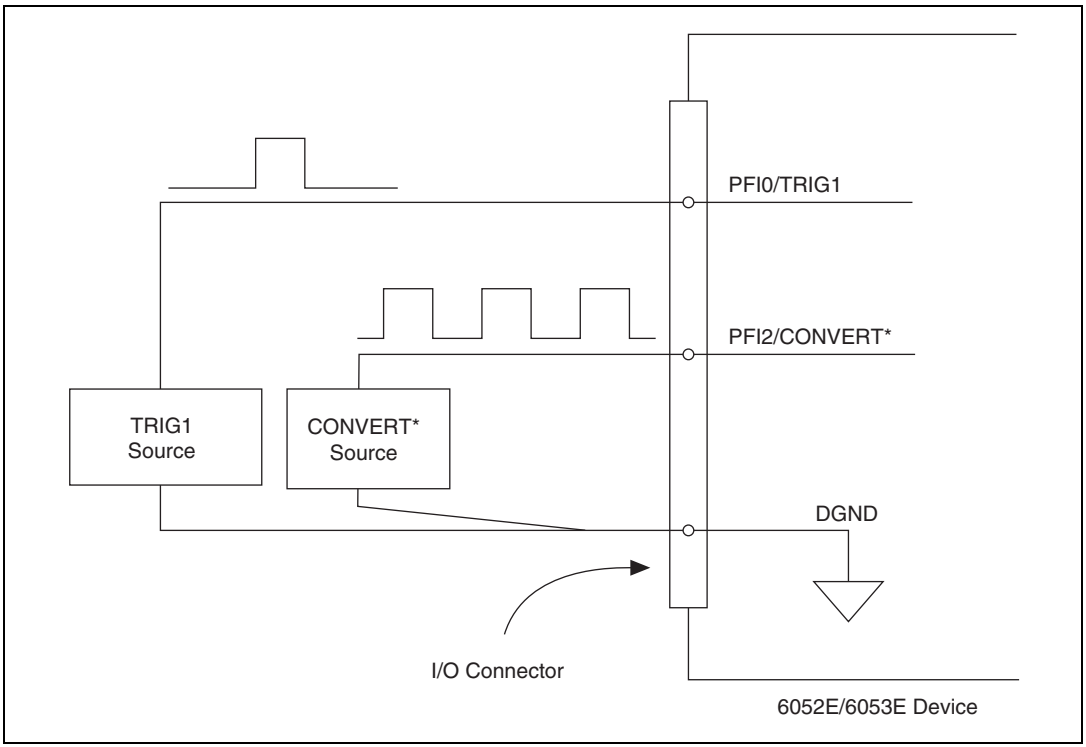


Figure 4-11. Timing I/O Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software-selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI signal for edge or level detection as well as for polarity selection. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection

will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse width requirements imposed by the PFIs themselves, but there can be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-12. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-13 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures is included later in this chapter.

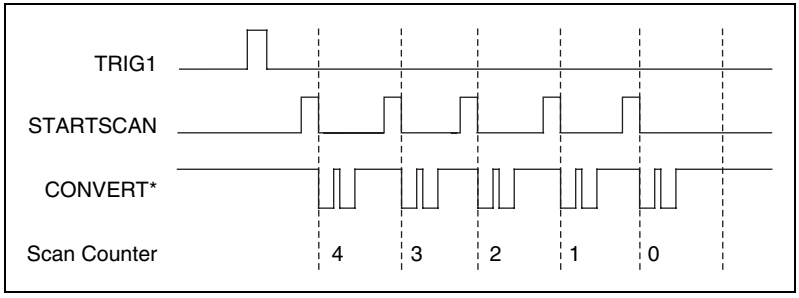


Figure 4-12. Typical Posttriggered Acquisition

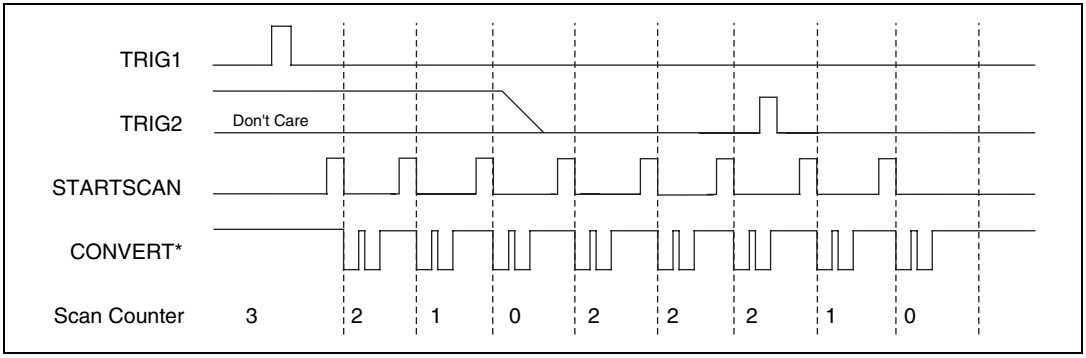


Figure 4-13. Typical Pretriggered Acquisition

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-14 shows the timing for the SCANCLK signal.

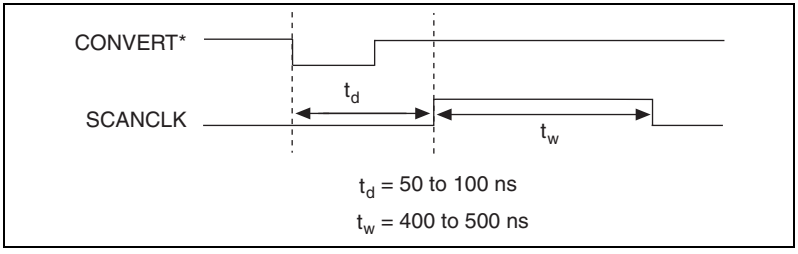


Figure 4-14. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-15 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

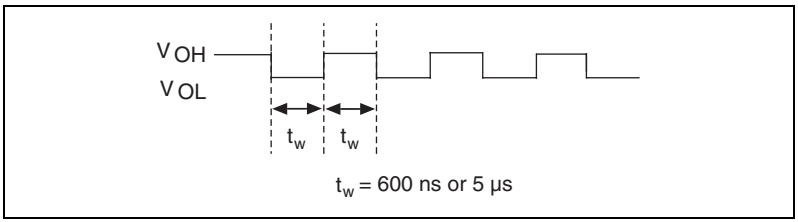


Figure 4-15. EXTSTROBE* Signal Timing

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-12 and 4-13 for the relationship of TRIG1 to the DAQ sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions. See Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a DAQ sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-16 and 4-17 show the input and output timing requirements for the TRIG1 signal.

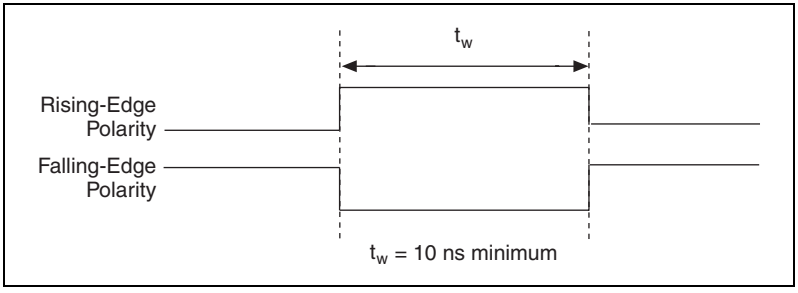


Figure 4-16. TRIG1 Input Signal Timing

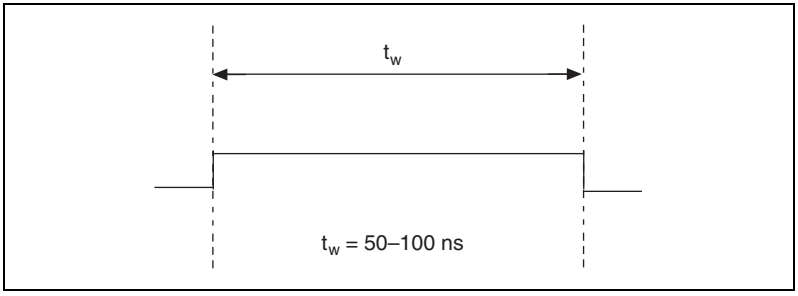


Figure 4-17. TRIG1 Output Signal Timing

The device also uses the TRIG1 signal to initiate pretriggered DAQ operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-13 for the relationship of TRIG2 to the DAQ sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device will acquire a fixed number of scans and the acquisition will stop. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-18 and 4-19 show the input and output timing requirements for the TRIG2 signal.

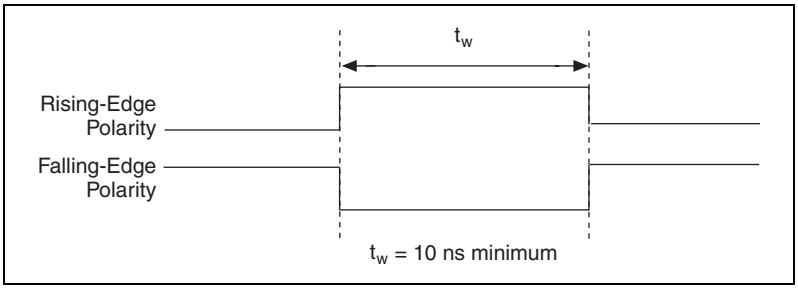


Figure 4-18. TRIG2 Input Signal Timing

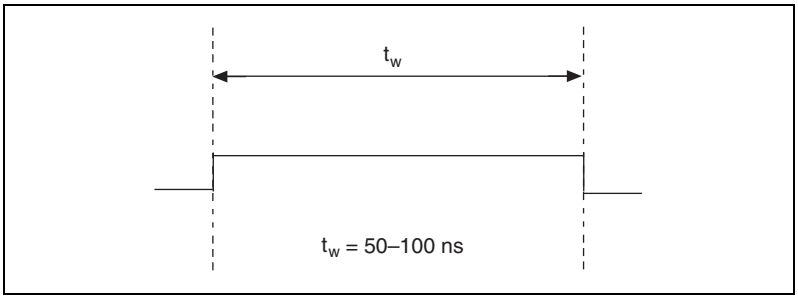


Figure 4-19. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-12 and 4-13 for the relationship of STARTSCAN to the DAQ sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter starts if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress.

STARTSCAN will be deasserted t_{off} after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-20 and 4-21 show the input and output timing requirements for the STARTSCAN signal.

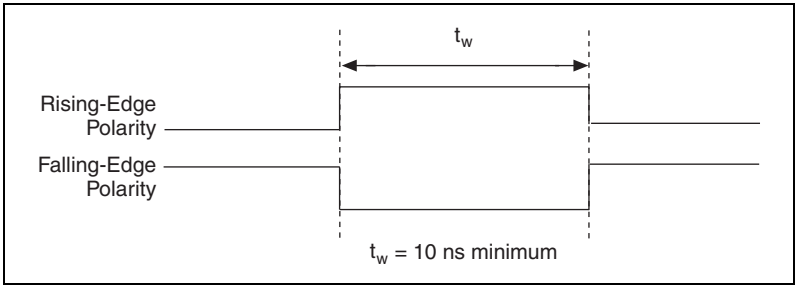


Figure 4-20. STARTSCAN Input Signal Timing

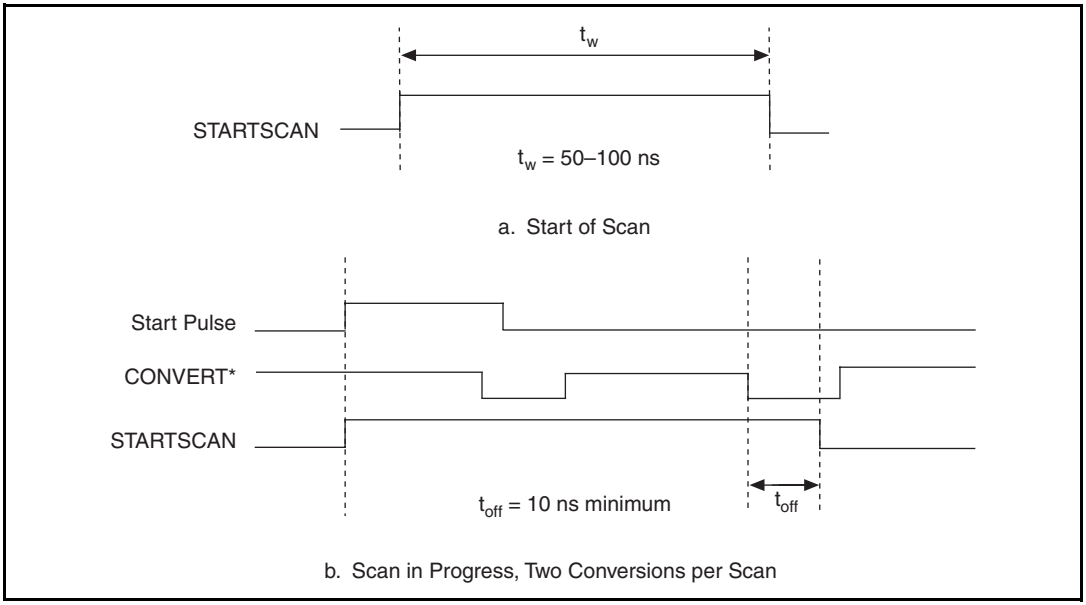


Figure 4-21. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on your device internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence can be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-12 and 4-13 for the relationship of CONVERT* to the DAQ sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-22 and 4-23 show the input and output timing requirements for the CONVERT* signal.

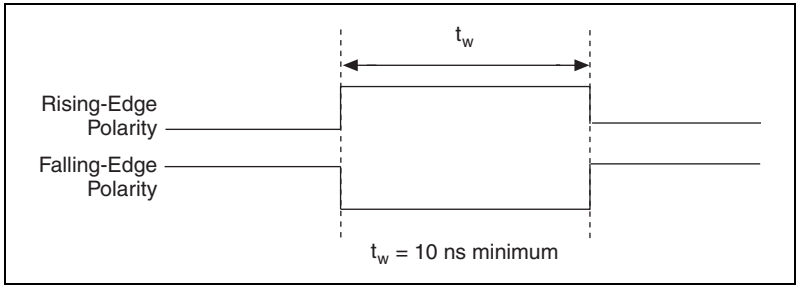


Figure 4-22. CONVERT* Input Signal Timing

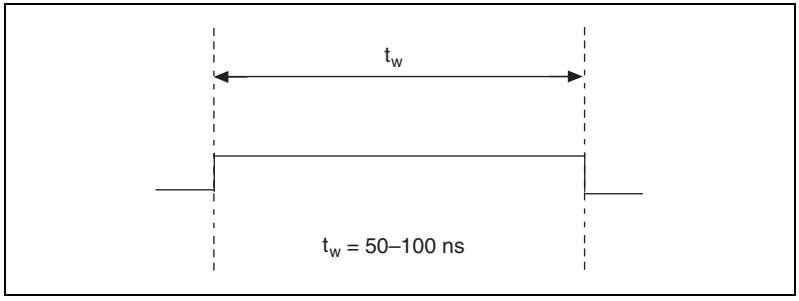


Figure 4-23. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The sample interval counter on the 6052E/6053E normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence can be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-24 shows the timing requirements for the SISOURCE signal.

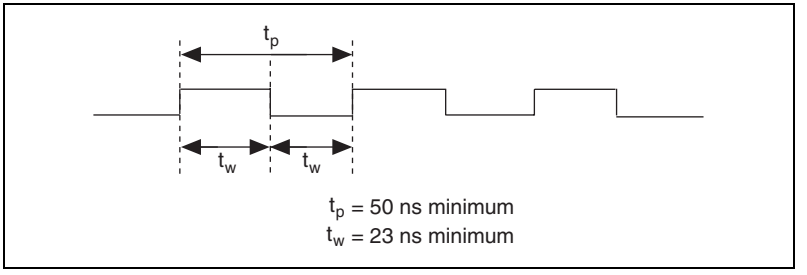


Figure 4-24. SISOURCE Signal Timing

Waveform Generation Timing Connections

The analog group defined for your PCI E Series device is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-25 and 4-26 show the input and output timing requirements for the WFTRIG signal.

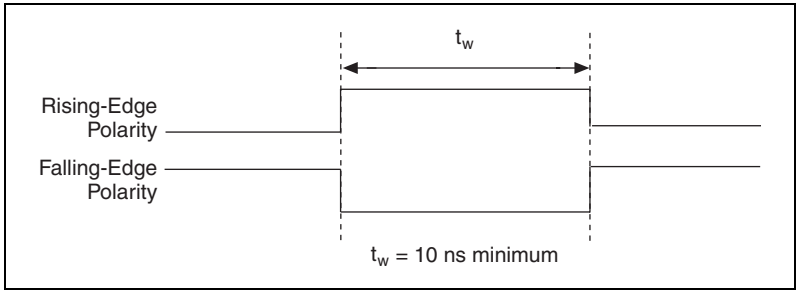


Figure 4-25. WFTRIG Input Signal Timing

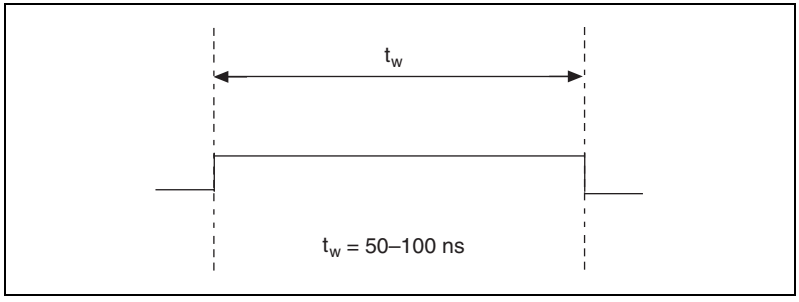


Figure 4-26. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to tri-state at startup.

Figures 4-27 and 4-28 show the input and output timing requirements for the UPDATE* signal.

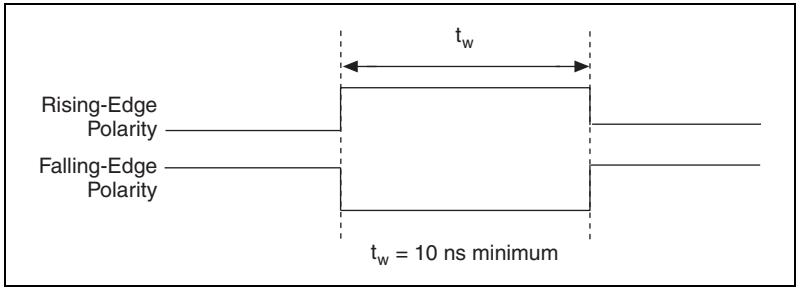


Figure 4-27. UPDATE* Input Signal Timing

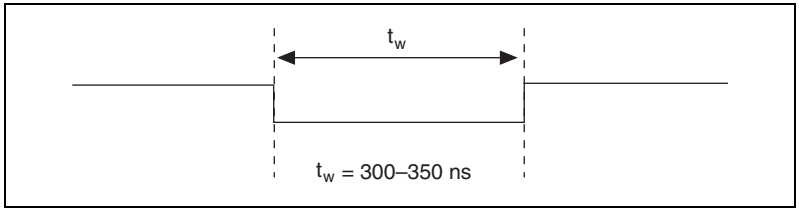


Figure 4-28. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The 6052E/6053E UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

When using an external UPDATE* signal, you must supply at least one more external update pulse than the number of points that you want to generate. This is necessary for proper hardware operation, otherwise the device does not indicate that the waveform generation is complete.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-29 shows the timing requirements for the UISOURCE signal.

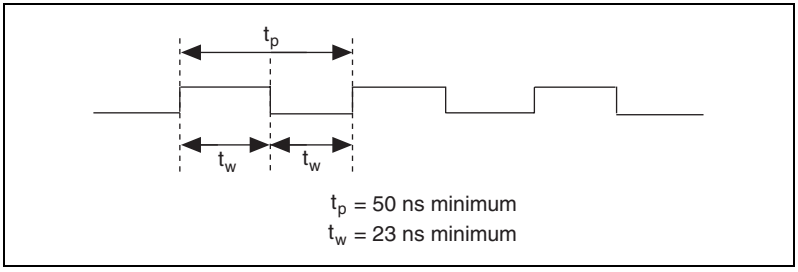


Figure 4-29. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This output is set to tri-state at startup.

Figure 4-30 shows the timing requirements for the GPCTR0_SOURCE signal.

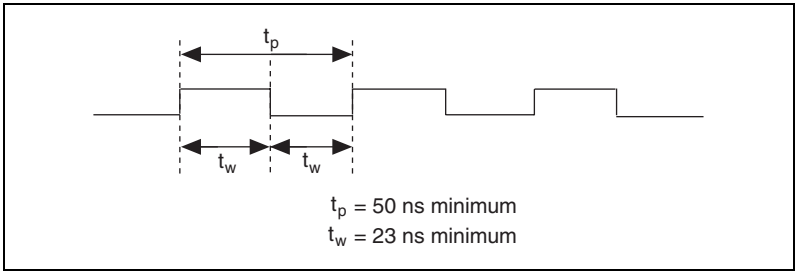


Figure 4-30. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-31 shows the timing requirements for the GPCTR0_GATE signal.

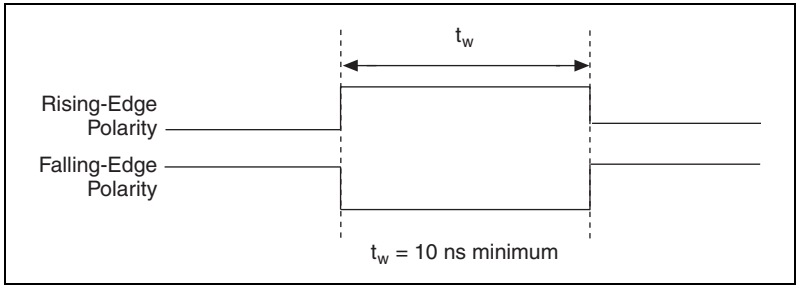


Figure 4-31. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-32 shows the timing of the GPCTR0_OUT signal.

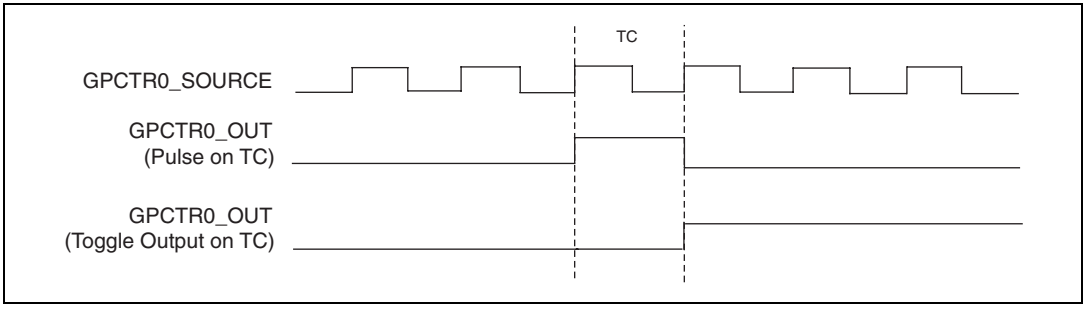


Figure 4-32. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-33 shows the timing requirements for the GPCTR1_SOURCE signal.

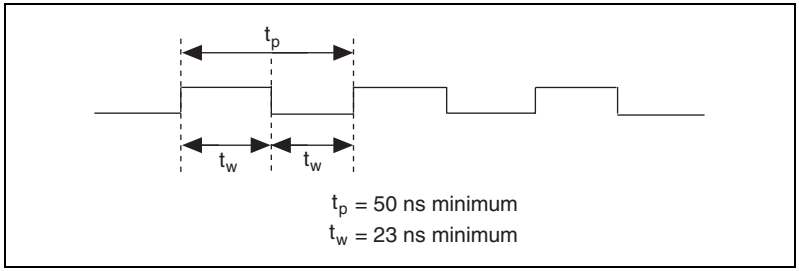


Figure 4-33. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-34 shows the timing requirements for the GPCTR1_GATE signal.

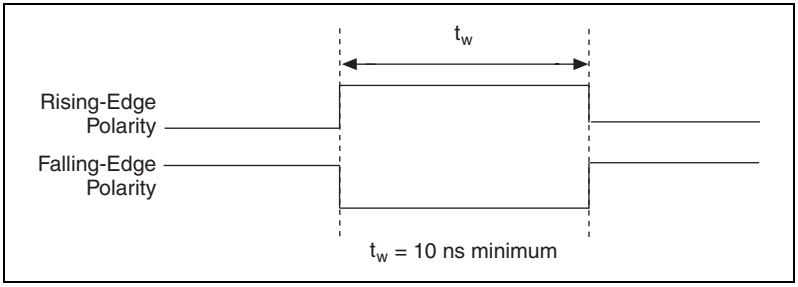


Figure 4-34. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-35 shows the timing requirements for the GPCTR1_OUT signal.

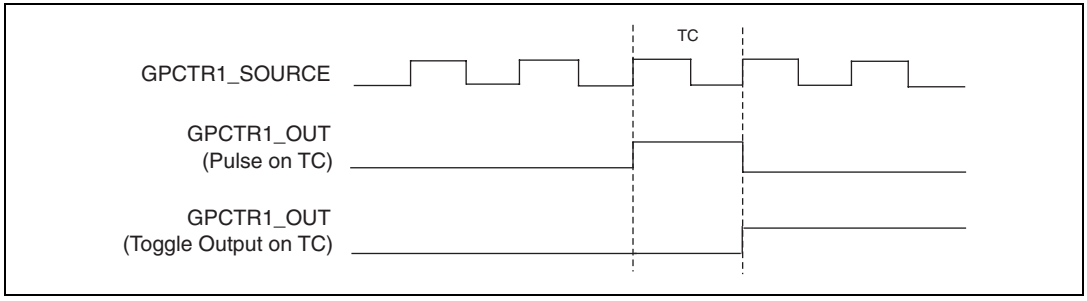


Figure 4-35. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-36 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of your device.

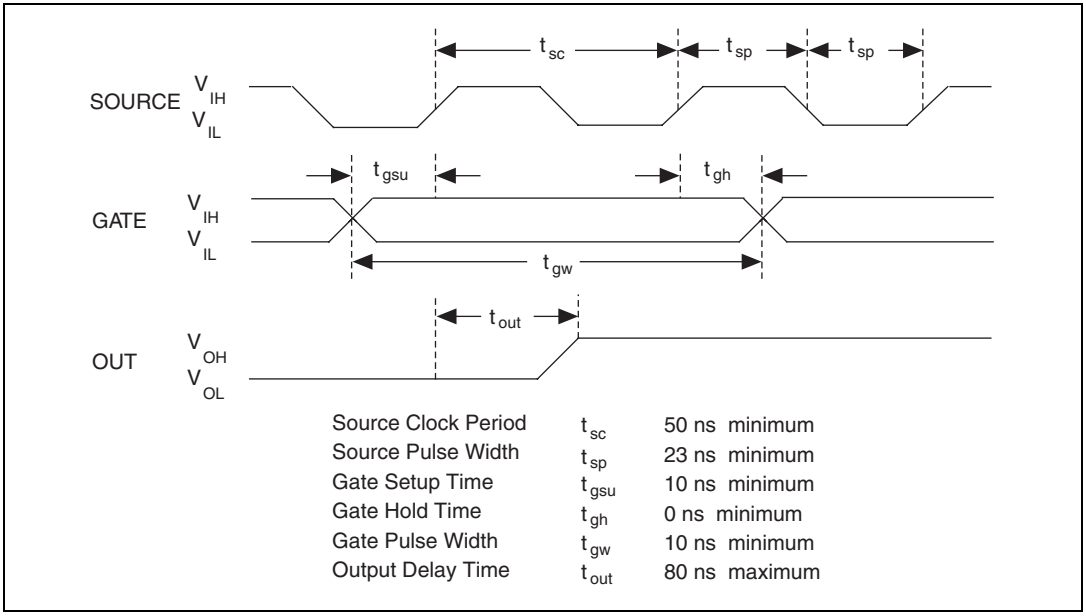


Figure 4-36. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-36 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. If the counter was programmed to count falling edges, the source signal would be inverted and referenced to the falling edge of the source signal in Figure 4-36.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on your device. Figure 4-36 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-36. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the 6052E/6053E. Figure 4-36 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal, generated from the 6052E/6053E device frequency generator, is available only as an output on the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to tri-state at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with your device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to analog input signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the device. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PCI DAQ system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to your device:

- Separate 6052E/6053E device signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the 6052E/6053E device signal lines if they run in parallel paths at a close distance.
  To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the application note, *Field Wiring and Noise Consideration for Analog Signals,* available from National Instruments.

5

Calibration

This chapter discusses the calibration procedures for your device. If you are using the NI-DAQ device driver, that software includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the 6052E/6053E devices, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for all but the most forgiving applications. If you do not calibrate your device, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

Your device is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

Your device can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

Your device has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your device at an extreme temperature or if the onboard reference has not been measured for a year or more, you can wish to externally calibrate your device.

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your device by calling the NI-DAQ calibration function.

To externally calibrate your device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

Other Considerations

The CalDACs adjust the gain error of each analog output channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the analog output gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the analog output channel either in software or with external hardware. See Appendix A, *Specifications*, for analog output gain error information.

Gain error and offset error are temperature dependent. Take care to power on your 6052E/6053E for the recommended warmup time in a stable temperature environment before calibrating the device. Refer to Appendix A, *Specifications*, to determine the warmup time. The device should be calibrated at the temperature in which it will operate.

A

Specifications

This appendix lists the specifications of the 6052E/6053E devices. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels

PCI-6052E ..... 16 single-ended or 8 differential (software selectable)

PCI-6053E ..... 64 single-ended or 32 differential (software selectable)

Type of ADC..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Max sampling rate..... 333 kS/s guaranteed

Input signal ranges

Device Gain (Software Selectable)	Device Range (Software Selectable)	
	Bipolar	Unipolar
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

6052E/6053E Accuracy Information

Nominal Range (V)		Absolute Accuracy							Relative Accuracy	
		% of Reading			Offset	Noise + Quantization (µV)		Temp Drift	Resolution (µV)	
Positive FS	Negative FS	24 Hours	90 Days	1 Year	(µV)	Single Pt.	Avg.	(%/°C)	Single Pt.	Avg.
10	–10	0.0304	0.0312	0.0321	1067	981	87.0	0.0006	1145	115
5	–5	0.0054	0.0062	0.0071	536	491	43.5	0.0001	573	57.3
2.5	–2.5	0.0304	0.0312	0.0321	271	245	21.7	0.0006	286	28.6
1	–1	0.0304	0.0312	0.0321	111	98.1	8.7	0.0006	115	11.5
0.5	–0.5	0.0304	0.0312	0.0321	58.1	56.2	5.0	0.0006	66.3	6.6
0.25	–0.25	0.0304	0.0312	0.0321	31.6	32.8	3.0	0.0006	39.2	3.9
0.1	–0.1	0.0304	0.0312	0.0321	15.6	22.4	2.1	0.0006	27.7	2.8
0.05	–0.05	0.0304	0.0312	0.0321	10.3	19.9	1.9	0.0006	25.3	2.5
10	0	0.0054	0.0062	0.0071	536	491	43.5	0.0001	573	57.3
5	0	0.0304	0.0312	0.0321	271	245	21.7	0.0006	286	28.6
2	0	0.0304	0.0312	0.0321	111	98.1	8.7	0.0006	115	11.5
1	0	0.0304	0.0312	0.0321	58.1	56.2	5.0	0.0006	66.3	6.6
0.5	0	0.0304	0.0312	0.0321	31.6	39.8	3.0	0.0006	48.2	3.9
0.2	0	0.0304	0.0312	0.0321	15.6	22.4	2.1	0.0006	27.7	2.8
0.1	0	0.0304	0.0312	0.0321	10.3	19.9	1.9	0.0006	25.3	2.5

Note: Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

Input coupling.....DC

Max working voltage
(signal + common-mode).....Each input should remain within ±11 V of ground

Overvoltage protection .....±25 V powered on, ±15 V powered off

Inputs protected
- PCI-6052E ..... ACH<0..15>, AISENSE
- PCI-6053E ..... ACH<0..63>, AISENSE, AISENSE2

FIFO buffer size ..... 512 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather

Configuration memory size ..... 512 words

Transfer Characteristics

Relative accuracy ..... ±1.5 LSB typ, ±3.0 LSB max

DNL ..... ±0.5 LSB typ, ±1.0 LSB max

No missing codes ..... 16 bits, guaranteed

Offset error
- Pregain error after calibration ..... ±1.0 µV max
- Pregain error before calibration ..... ±2.6 mV max
- Postgain error after calibration ..... ±76 µV
- Postgain error before calibration ..... ±82 mV

Gain error (relative to calibration reference)
- After calibration (gain = 1) ..... ±30.5 ppm of reading max
- Before calibration ..... ±22,000 ppm of reading max

Gain ≠ 1 with gain error adjusted to 0 at gain = 1 ..... ±200 ppm of reading max

Amplifier Characteristics

Input impedance
- Normal powered on ..... 100 GΩ in parallel with 100 pF
- Powered off ..... 820 Ω min
- Overload ..... 820 Ω min

Input bias current ..... ±200 pA

Input offset current .....±100 pA

CMRR, DC to 60 Hz

Gain = 0.5 .....92 dB

Gain = 1 .....97 dB

Gain = 2 .....101 dB

Gain = 5 .....104 dB

Gain ≥ 10 .....105 dB

Dynamic Characteristics

Bandwidth

Small signal (–3 dB).....480 kHz

Large signal (1% THD).....500 kHz

Dynamic range.....87 dB, ±10 V input, gain 0.5 to 5
83 dB, gain 10

Settling time for full-scale step

±16 LSB .....3 µs typical

±4 LSB .....4 µs max

±2 LSB .....5 µs max, gain 0.5 to 10
8 µs max, gain 20 to 50
10 µs max, gain 100

±1 LSB .....10 µs max, gain 0.5 to 5
15 µs max, gain 10 to 100

±1/2 LSB .....20 µs typical

System noise (including quantization noise)

Gain	Noise
0.5 to 5	0.95 LSB rms
10	1.1 LSB rms
20	1.3 LSB rms
50	2.3 LSB rms
100	4.2 LSB rms

Crosstalk, DC to 100 kHz

Adjacent channels ..... –75 dB

Other channels ..... ≤ –90 dB

Stability

Recommended warm-up time

PCI/PXI-6052E/6053E ..... 15 minutes

Offset temperature coefficient

Pregain ..... ±4 µV/°C

Bipolar postgain ..... ±120 µV/°C

Unipolar postgain ..... ±30 µV/°C

Gain temperature coefficient ..... ±17 ppm/°C

Onboard calibration reference

Level ..... 5.000 V (±1.0 mV)
(over full operating temperature, actual value stored in EEPROM)

Temperature coefficient ..... ±0.6 ppm/°C max

Long-term stability ..... ±6 ppm / $\sqrt{1{,}000\text{h}}$

Analog Output

Output Characteristics

Number of channels ..... 2 voltage

Resolution ..... 16 bits, 1 in 16,536

Max update rate ..... 333 kS/s

Type of DAC ..... Double buffered, multiplying

FIFO buffer size ..... 2,048 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather

PXI-6052E/6053E Accuracy Information

Nominal Range (V)		Absolute Accuracy				
		% of Reading			Offset	Temp Drift
Positive FS	Negative FS	24 Hrs	90 Days	1 Year	(μV)	(%/°C)
10	–10	0.0044%	0.0052%	0.0061%	±798 μV	0.0001%
10	0	0.0044%	0.0052%	0.0061%	±569 μV	0.0001%

Absolute Accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage)

Note: Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.

Transfer Characteristics

Relative accuracy (INL)

After calibration.....±0.35 LSB typ, ±1.0 LSB max

Before calibration .....±4 LSB max

DNL

After calibration.....±0.5 LSB typ, ±1.0 LSB max

Before calibration .....±3 LSB max

Monotonicity .....16 bits, guaranteed after calibration

Offset error

After calibration.....±305 μV max

Before calibration .....±17 mV max

Gain error (relative to internal reference)

After calibration.....±30.5 ppm of output max

Before calibration .....±9,000 ppm of output max

Gain error
(relative to external reference).....+0% to +0.5% of output max, not adjustable

Voltage Output

Ranges ..... ±10 V, 0 to 10 V, ± EXTREF, 0 to EXTREF (software-selectable)

Output coupling ..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state ..... ±0.020 V max

External reference input

- Range ..... ±11 V
- Overvoltage protection ..... ±25 V powered on, ±15 V powered off
- Input impedance ..... 10 kΩ
- Bandwidth (–3 dB) ..... 3 kHz
- Slew rate ..... 0.3 V/µs

Dynamic Characteristics

Settling time for full-scale step ..... 3.5 µs to ±1.0 LSB accuracy

Settling time for half-scale step ..... 3.0 µs to ±1.0 LSB accuracy

Slew rate ..... 15 V/µs

Noise ..... 60 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

- Magnitude ..... 10 mV
- Duration ..... 1 µs

Stability

Offset temperature coefficient ..... ±35 µV/°C

Gain temperature coefficient

Internal reference.....±6.5 ppm/°C

External reference.....±5 ppm/°C

Onboard calibration reference

Level.....5.000 V (±1.0 mV)
(over full operating temperature, actual value stored in EEPROM)

Temperature coefficient.....±0.6 ppm/°C max

Long-term stability.....±6 ppm/$\sqrt{1{,}000\text{h}}$

Digital I/O

Number of channels.....8 input/output

Compatibility.....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (Vin = 0 V)	—	–320 µA
Input high current (Vin = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state.....Input (High-Z)

Data transfers.....Programmed I/O

Timing I/O

Number of channels.....2 up/down counter/timers, 1 frequency scaler

Resolution

Counter/timers.....24 bits

Frequency scalers.....4 bits

Compatibility.....TTL/CMOS

Base clocks available
- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scalers..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration..... 10 ns in edge-detect mode

Min gate pulse duration..... 10 ns in edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes..... Scatter-gather

Triggers

Analog Trigger

Source
- PCI-6052E ..... ACH<0..15>, PFI0/TRIG1
- PCI-6053E ..... ACH<0..63>, PFIO/TRIG1

Level..... ± full-scale, internal; ±10 V, external

Slope..... Positive or negative (software-selectable)

Resolution ..... 12 bits, 1 in 4,096

Hysteresis ..... Programmable

Bandwidth (–3 dB)..... 700 kHz internal, 700 kHz external

External input (PFI0/TRIG1)
- Impedance ..... 10 k Ω
- Coupling..... DC

Protection.....–0.5 to Vcc + 0.5 V when configured as a digital signal
±35 V when configured as an analog trigger signal or disabled
±35 V powered off

Accuracy.....±1.0% of full scale range max

Digital Trigger

Compatibility.....TTL

Response.....Rising or falling edge

Pulse width.....10 ns min

RTSI

Trigger lines

PCI/PXI-6052E/6053E.....7

Clock line.....1

Bus Interface

Type

PCI/PXI-6052E/6053E.....Master, Slave

DAQPad-6052E for 1394.....Master, Slave, Asynchronous

Power Requirement

Power available at I/O connector.....+4.65 VDC to +5.25 VDC at 1 A

PCI/PXI-6052E/6053E
+5 VDC (±5%).....1.3 A
(does not include current drawn from 5 V fuse on I/O connector)

DAQPad-6052E for 1394
9–24 VDC.....20W

Physical

Dimensions (not including connectors)

- PCI-6052E/6053E ..... 17.5 by 10.6 cm (6.9 by 4.2 in.)
- PXI-6052E/6053E ..... 16 by 10 cm (6.3 by 3.9 in.)
- DAQPad-6052E for 1394 ..... 14.6 by 21.6 by 3.8 cm (5.8 by 8.4 by 1.5 in.)

I/O connector

- PCI-6052E ..... 68-pin male SCSI-II type
- PCI-6053E ..... 100-pin female 0.05 D-type

Environment

Operating temperature ..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Relative humidity ..... 5% to 90% noncondensing

B

Custom Cabling and Optional Connectors

This appendix describes the various cabling and connector options.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines can be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The following list gives recommended part numbers for connectors that mate to the I/O connector on your 6052E/6053E device.

Mating connectors and a backshell kit for making custom 68-pin cables are available from National Instruments (part number 776832-01).

- Honda 68-position, solder cup, female connector (part number PCS-E68FS)
- Honda backshell (part number PCS-E68LKPA)

Optional Connectors

Refer to Figure 4-1, *I/O Connector Pin Assignment for 6052E/6053E.* Figure 4-1 shows the pin assignments for the 68-pin connector. This connector is available when you use the SH6868EP or R6868 cable assemblies with the 6052E device. This connector is also one of two 68-pin connectors that is available when you use the SH1006868 cable assembly with the PCI/PXI-6053E.

Figure B-1 shows the pin assignments for the 68-pin extended analog input connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the PCI/PXI-6053E.

ACH 24	34	68	ACH 16
ACH 17	33	67	ACH 25
ACH 18	32	66	ACH 26
ACH 27	31	65	ACH 19
ACH 20	30	64	ACH 28
ACH 21	29	63	ACH 29
ACH 30	28	62	ACH 22
ACH 23	27	61	ACH 31
ACH 32	26	60	ACH 40
ACH 41	25	59	ACH 33
ACH 34	24	58	ACH 42
ACH 35	23	57	ACH 43
AIGND	22	56	AISENSE2
ACH 44	21	55	ACH 36
ACH 37	20	54	ACH 45
ACH 38	19	53	ACH 46
ACH 47	18	52	ACH 39
ACH 48	17	51	ACH 56
ACH 49	16	50	ACH 57
ACH 58	15	49	ACH 50
ACH 51	14	48	ACH 59
ACH 52	13	47	ACH 60
ACH 61	12	46	ACH 53
ACH 54	11	45	ACH 62
ACH 55	10	44	ACH 63
N/C	9	43	N/C
N/C	8	42	N/C
N/C	7	41	N/C
N/C	6	40	N/C
N/C	5	39	N/C
N/C	4	38	N/C
N/C	3	37	N/C
N/C	2	36	N/C
N/C	1	35	N/C

Figure B-1. 68-Pin Extended Analog Input Connector Pin Assignments

Figure B-2 shows the pin assignments for the 50-pin connector. This connector is available when you use the SH6850 or R6850 cable assemblies. It is also one of the two 50-pin connectors available when you use the R1005050 cable assembly with the PCI/PXI-6053E.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5 V
+5 V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-2. 50-Pin Connector Pin Assignments

Figure B-3 shows the pin assignments for the 50-pin extended analog input connector. This is the other 50-pin connector available when you use the R1005050 cable assembly with the PCI/PXI-6053E.

ACH16	1	2	ACH24
ACH17	3	4	ACH25
ACH18	5	6	ACH26
ACH19	7	8	ACH27
ACH20	9	10	ACH28
ACH21	11	12	ACH29
ACH22	13	14	ACH30
ACH23	15	16	ACH31
ACH32	17	18	ACH40
ACH33	19	20	ACH41
ACH34	21	22	ACH42
ACH35	23	24	ACH43
AISENSE2	25	26	AIGND
ACH36	27	28	ACH44
ACH37	29	30	ACH45
ACH38	31	32	ACH46
ACH39	33	34	ACH47
ACH48	35	36	ACH56
ACH49	37	38	ACH57
ACH50	39	40	ACH58
ACH51	41	42	ACH59
ACH52	43	44	ACH60
ACH53	45	46	ACH61
ACH54	47	48	ACH62
ACH55	49	50	ACH63

Figure B-3. 50-Pin Extended Analog Input Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your device.

General Information

What is the DAQ-STC?

The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by National Instruments and is the backbone of the E Series devices. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

What does sampling rate mean to me?

It means that this is the fastest you can acquire data on your device and still achieve accurate results. For example, the PCI-6052E/6053E has a sampling rate of 333 kS/s. This sampling rate is aggregate: one channel at 333 kS/s or two channels at 166.5 kS/s per channel illustrates the relationship. Notice, however, that the PCI-6052E/6053E has settling times that vary with gain and accuracy. See Appendix A, *Specifications*, for exact specifications.

What type of 5 V protection do the PCI-6052E/6053E, PXI-6052E/6053E, and DAQPad-6052E have?

The PCI-6052E/6053E, PXI-6052E/6053E, and DAQPad-6052E for 1394 have 5 V lines equipped with a self-resetting 1 A fuse.

Installation and Configuration

How do you set the base address for a PCI-6052E/6053E or PXI-6052E/6053E?

The base address of the PCI-6052E/6053E and PXI-6052E/6053E is assigned automatically through the PCI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring my device?

The PCI-6052E/6053E and PXI-6052E/6053E are jumperless and switchless.

Which National Instruments document should I read first to get started using DAQ software?

Your NI-DAQ or application software release notes documentation is always the best starting place.

What version of NI-DAQ must I have to program my device?

You must have NI-DAQ version 6.5 or later for the PCI-6052E. The PXI-6052E requires NI-DAQ version 6.6 or later. The PCI/PXI-6053E require NI-DAQ version 6.9 or later.

What is Firewire?

Firewire and IEEE 1394 are the same thing. Firewire was the original name when the technology was developed by Apple. Later, Apple turned over the specification to the IEEE for standardization. Firewire is a registered trademark of Apple.

Can I use a 400 Mbyte/s 1394 device with a 100 Mbyte/s device?

Yes. However, the bus slows to the slowest speed. So, your 400 Mbytes/s 1394 device will operate faster if the 100 Mbytes/s device is removed from the bus.

How many devices can I hook up to a 1394 bus?

Up to 64 different devices, including the PC, may be attached to a single device.

Can I hook up the 1394 bus any way I want?

No. You can not have cycles in the bus cabling, and you must have fewer than 16 hops between devices.

What can I do to optimize the performance of my 1394 device?

There are several things that can be done to optimize the performance of your 1394 device. First, try to keep your bus running at the fastest speed possible by attaching only devices that are at least at fast as your 1394 device. If a 200 Mbytes/s device is added to the bus with your 400 Mbytes/s DAQ device, you will slow the entire bus down to 200 Mbytes/s. Second, minimize the maximum number of hops between the devices on the bus. The more hops you have the slower the bus will run. Finally, remember there is only a limited amount of bandwidth available on the bus. If you stream DV at 20 Mbytes/s, you will hurt your DAQ performance.

Will 1394 DAQ work with Windows 95?

No, Microsoft and National Instruments do *not* support Windows 95 and 1394.

Analog Input and Output

I'm using my device in differential analog input mode and I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check your ground reference connections. Your signal can be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the

frequency and nature of your output signal. See the *Analog Output Reglitch* section in Chapter 3, *Hardware Overview*, for more information about reglitching.

Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my device?

Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.
4. Initiate analog output waveform generation.

Timing and Digital I/O

What types of triggering can be hardware-implemented on my device?

Digital triggering is hardware-supported as well as analog triggering in hardware.

What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering,

selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO devices have a 20 MHz timebase. The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

Will the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the E Series and other devices; the counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on device without the DAQ-STC).

If you are using the NI-DAQ language interface or LabWindows/CVI, the answer is no, the counter/timer applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my E Series device, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using the NI-DAQ language interface or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution If you enable a PFI line for output, do *not* connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines can have pull up or pull down resistors connected to them as shown in Table 4-2, *I/O Connector Signal Descriptions*, and Table 4-3, *I/O Signal Summary*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-1 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high-impedance state.

D

Technical Support Resources

Web Support

National Instruments Web support is your first stop for help in solving installation, configuration, and application problems and questions. Online problem-solving and diagnostic resources include frequently asked questions, knowledge bases, product-specific troubleshooting wizards, manuals, drivers, software updates, and more. Web support is available through the Technical Support section of `www.ni.com`

NI Developer Zone

The NI Developer Zone at `ni.com/zone` is the essential resource for building measurement and automation systems. At the NI Developer Zone, you can easily access the latest example programs, system configurators, tutorials, technical news, as well as a community of developers ready to share their own techniques.

Customer Education

National Instruments provides a number of alternatives to satisfy your training needs, from self-paced tutorials, videos, and interactive CDs to instructor-led hands-on courses at locations around the world. Visit the Customer Education section of `www.ni.com` for online course schedules, syllabi, training centers, and class registration.

System Integration

If you have time constraints, limited in-house technical resources, or other dilemmas, you may prefer to employ consulting or system integration services. You can rely on the expertise available through our worldwide network of Alliance Program members. To find out more about our Alliance system integration solutions, visit the System Integration section of `www.ni.com`

Worldwide Support

National Instruments has offices located around the world to help address your support needs. You can access our branch office Web sites from the Worldwide Offices section of `www.ni.com`. Branch office web sites provide up-to-date contact information, support phone numbers, e-mail addresses, and current events.

If you have searched the technical support resources on our Web site and still cannot find the answers you need, contact your local office or National Instruments corporate. Phone numbers for our worldwide offices are listed at the front of this manual.

Glossary

Prefix	Meanings	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

%	percent
+	positive of, or plus
–	negative of, or minus
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
/	per
°	degree
Ω	ohm
$\sqrt{}$	square root of
+5 V	+5 VDC source signal

A

A	amperes
AC	alternating current
ACH	analog input channel signal
A/D	analog-to-digital
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
AI	analog input
AIGATE	analog input gate signal
AIGND	analog ground signal
AISENSE	analog sense signal
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions for a specific customer

B

BIOS	basic input/output system—BIOS functions are the fundamental level of any PC or compatible computer. BIOS functions embody the basic operations needed for successful use of the computer's hardware resources.
bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
common-mode noise	unwanted signals that appear in equal phase and amplitude on both the inverting and noninverting input in a differential measurement system. Ideally, but not completely in practice, the measurement device ignores this noise, because the measurement device is designed to respond to the difference between the inverting and noninverting inputs.
CONVERT*	convert signal
counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal

DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: $dB=20\log_{10}(V_1/V_2)$, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential mode
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an analog input FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
FREQ_OUT	frequency output signal
ft	feet

G

GATE	gate signal
GPCTR	general purpose counter
GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR0_OUT	general purpose counter 0 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general purpose counter 0 up down
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general purpose counter 1 up down

H

h	hour
hex	hexadecimal
Hz	hertz—the number of scans read or updates written per second

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry

L

LSB	least significant bit

M

m	meters
MB	megabytes of memory
MIO	multifunction I/O
MITE	MXI Interface to Everything—a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high-speed data transfers over the PCI bus.
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel

N

NC	normally closed, or not connected
NI-DAQ	National Instruments driver software for DAQ hardware
noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	programmable function input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general purpose counter 1 gate
PFI5/UPDATE*	PFI5/update

PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_ SOURCE	PFI8/general purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general purpose counter 0 gate
PGIA	programmable gain instrumentation amplifier
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
ppm	parts per million
pu	pullup

R

RAM	random-access memory
reglitch	circuitry used on analog outputs to generate uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum.
rms	root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude
RSE	referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.
RTD	resistance temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions

S

s	seconds
S	samples
SCANCLK	scan clock signal
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy PC environment
SE	single-ended—a term used to describe an analog input that is measured with respect to a common ground
settling time	the amount of time required for a voltage to reach its final value within specified limits
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
SOURCE	source signal
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
STARTSCAN	start scan signal
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count—the highest value of a counter
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
t_{out}	output delay time

THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage
thermocouple	a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TRIG	trigger signal
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic

U

UI	update interval
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
update	the output equivalent of a scan. One or more analog or digital output samples. Typically, the number of output samples in an update is equal to the number of channels in the output group. For example, one pulse from the update clock produces one update which sends one new sample to every analog output channel in the group.

V

V	volts
V_{DC}	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low

V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
Vrms	volts, root mean square

W

waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal

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